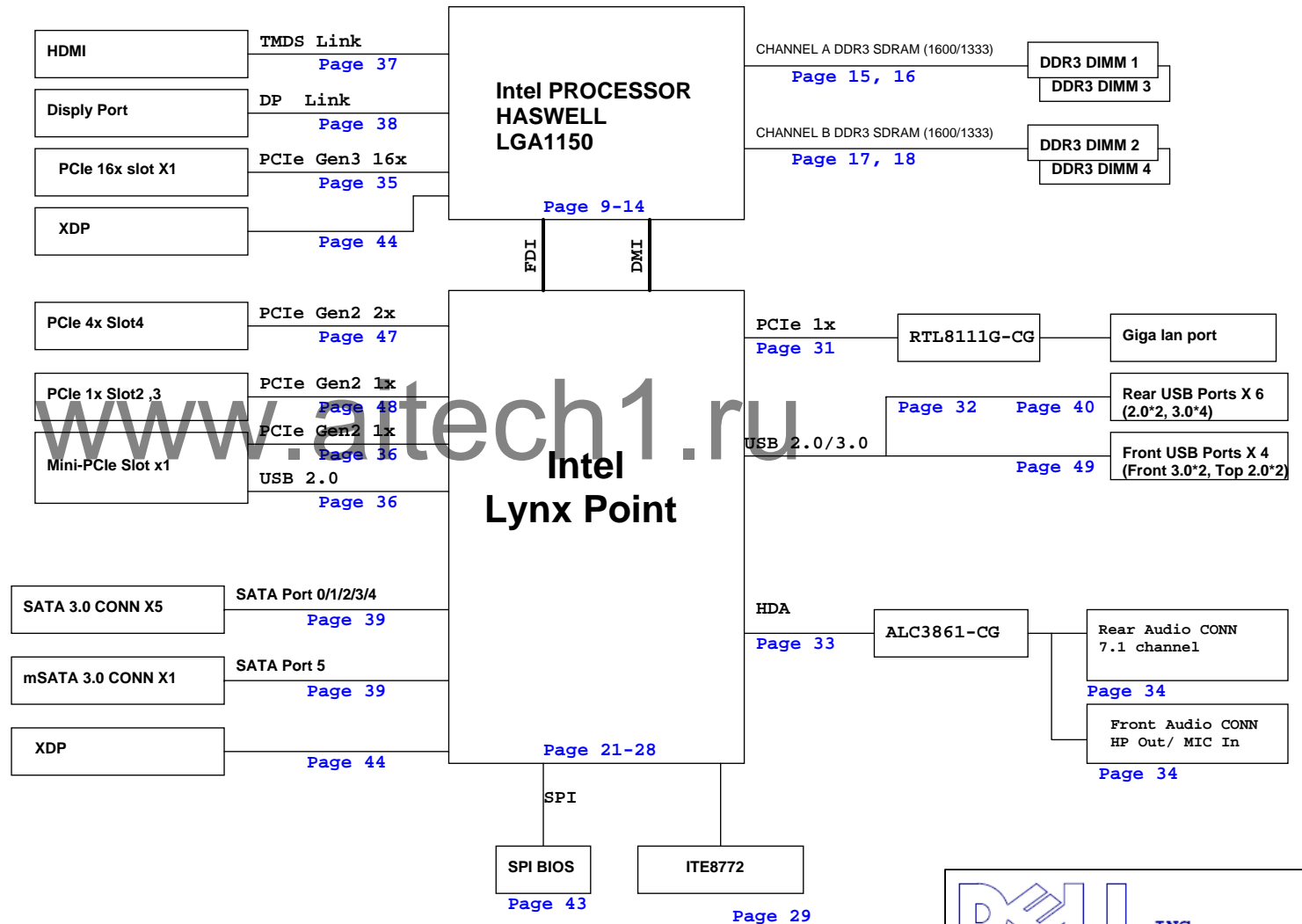


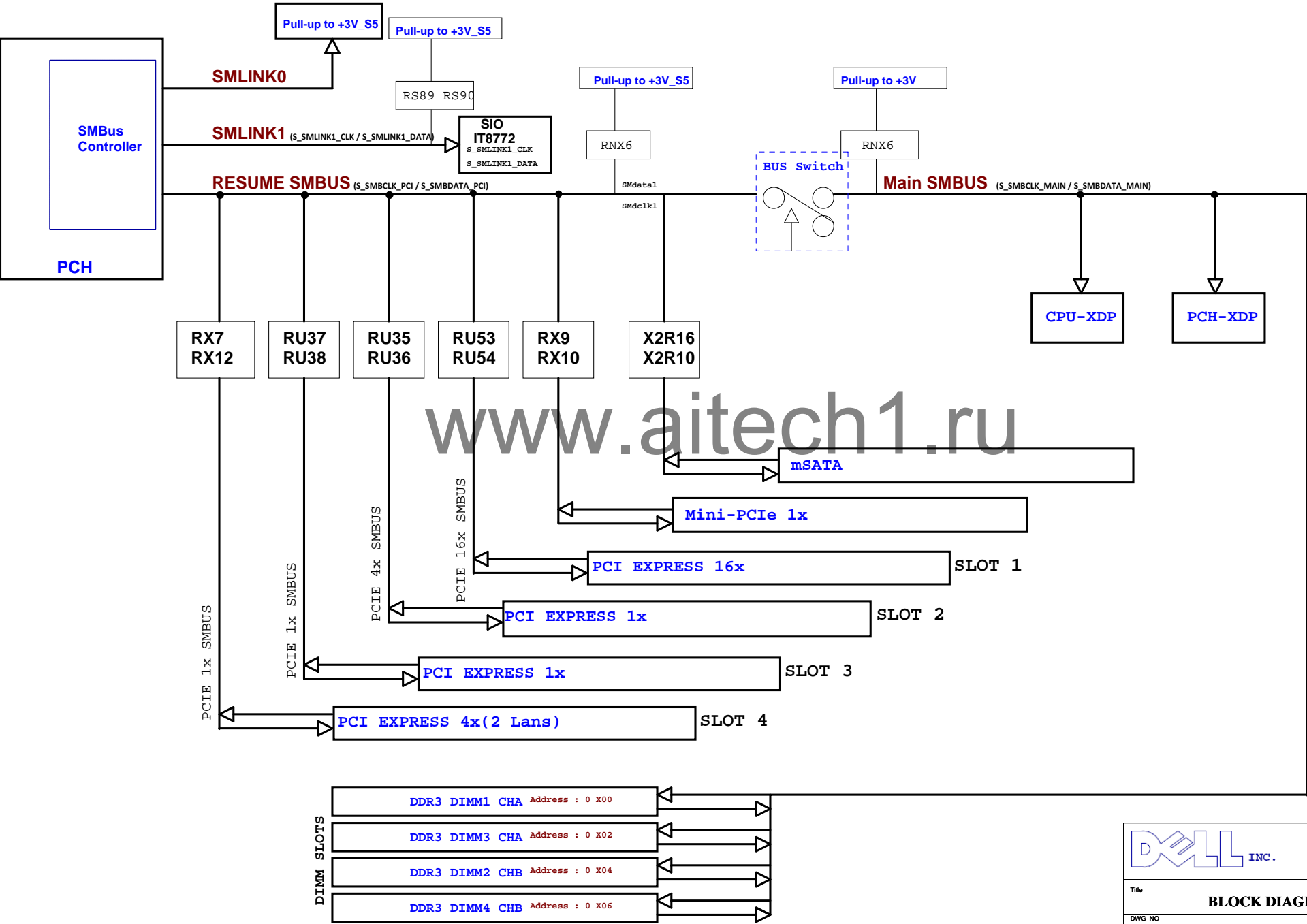
1. Index / Block diagram
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7. Strap/IRQ/IDSel Table
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- 33-34. Audio: ALC3861
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36. Mini PCIe
37. HDMI
38. Display port
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41. FAN
42. Serial / PS2 port
43. SPI-LPC DBG
44. XDP
45. EMI
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47. Slot4: PCIe 4x
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49. Front USB
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54. Power-4: Vcore PWM
55. Power-5: Vcore Driver
56. Power-6: DDR3
57. +5V\_DUAL/+5V\_DUAL\_USBKB

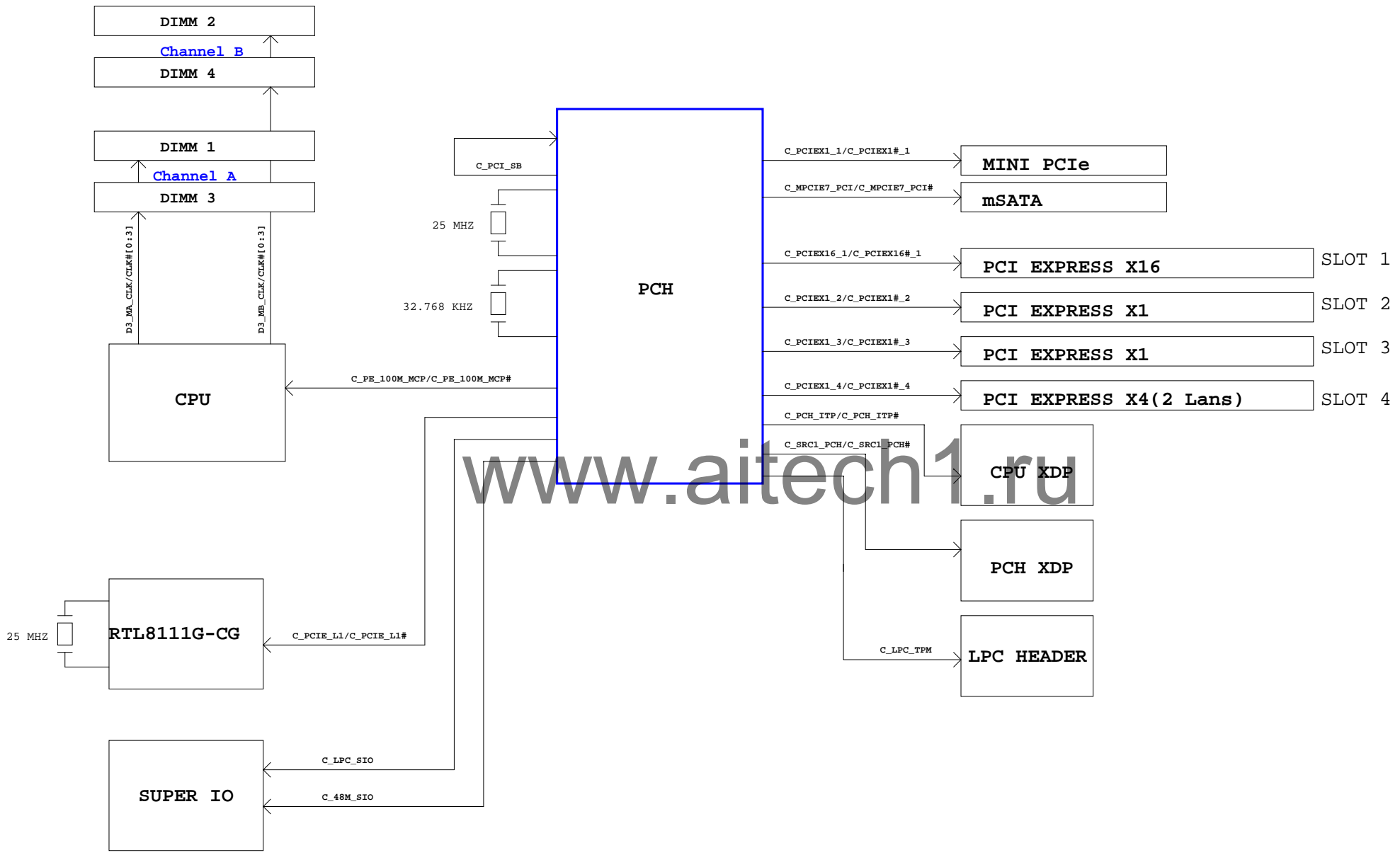
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VRD12.5 / VRM / Linear

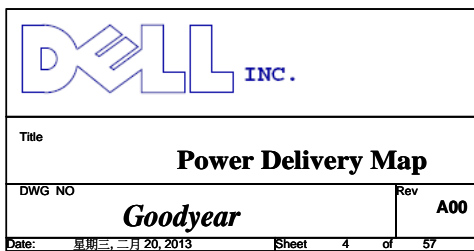
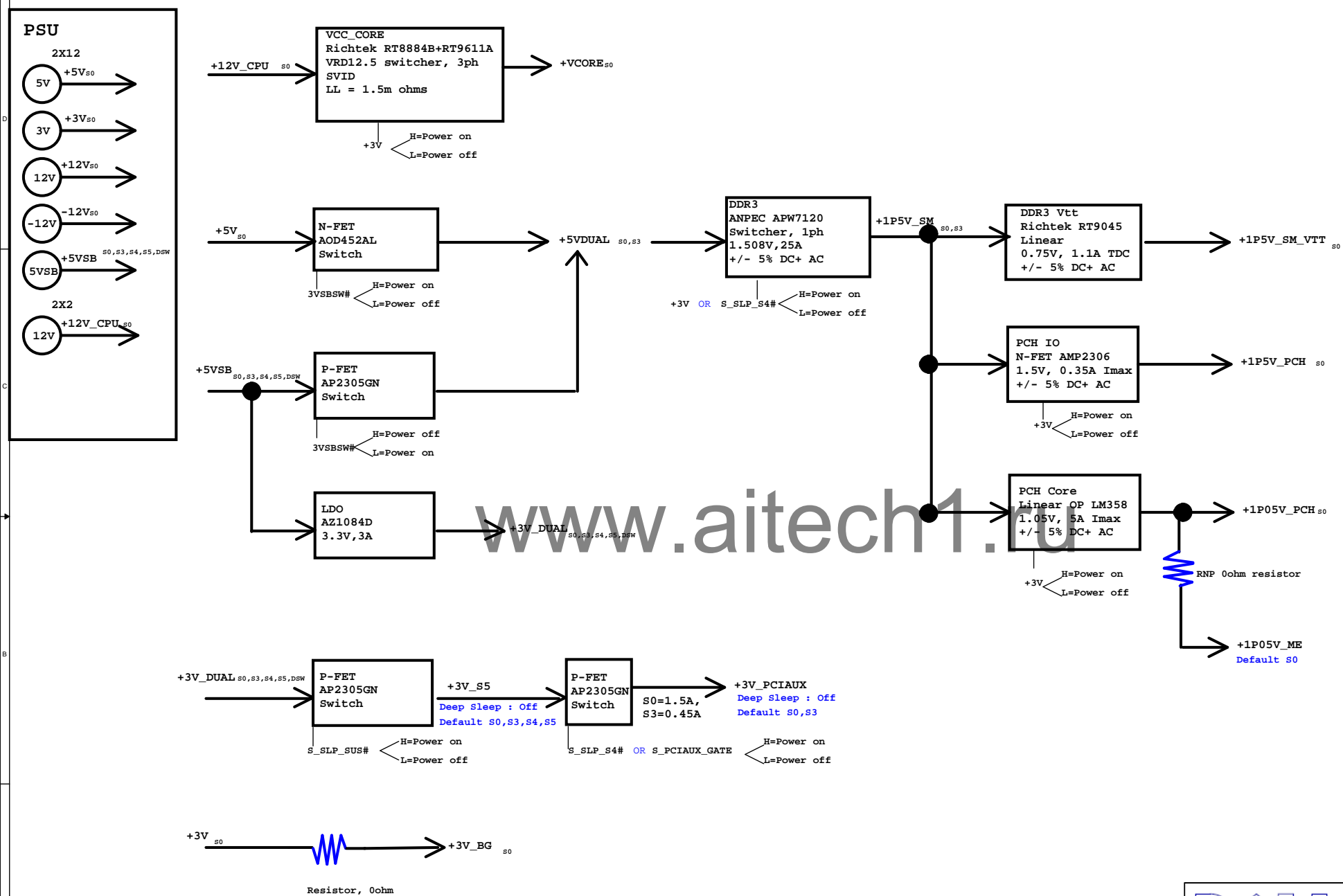


SMBUS DIAGRAM





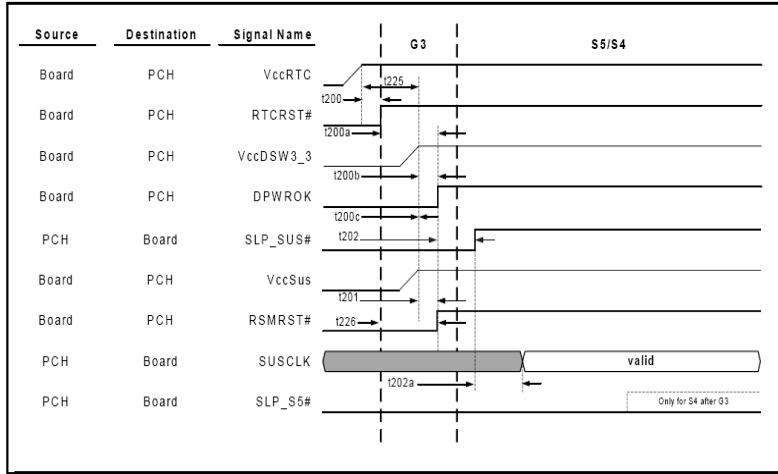
## POWER DELIVERY MAP



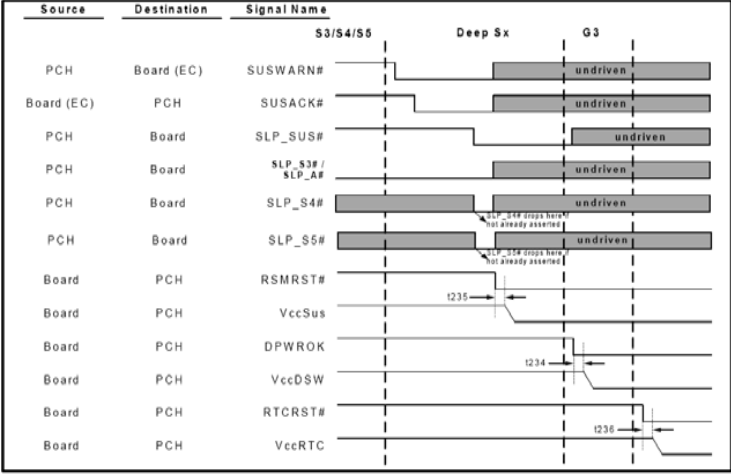


POWER ON Timing Diagram

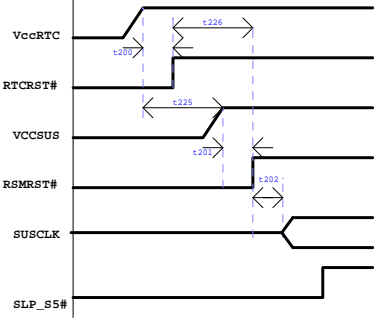
G3 --> S4/S5 (with Deep Sleep support)



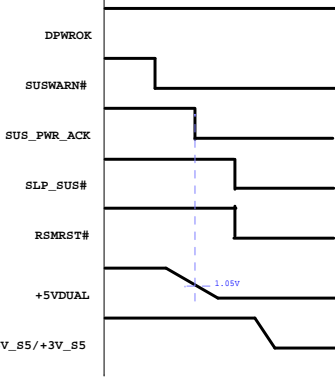
Sx --> Deep S4/S5 -->G3



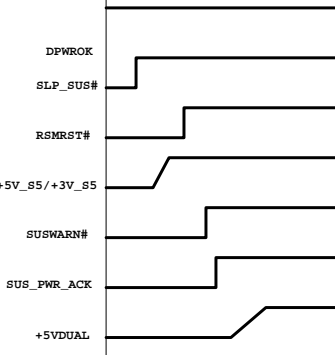
G3 to S4/S5 Timing Diagram



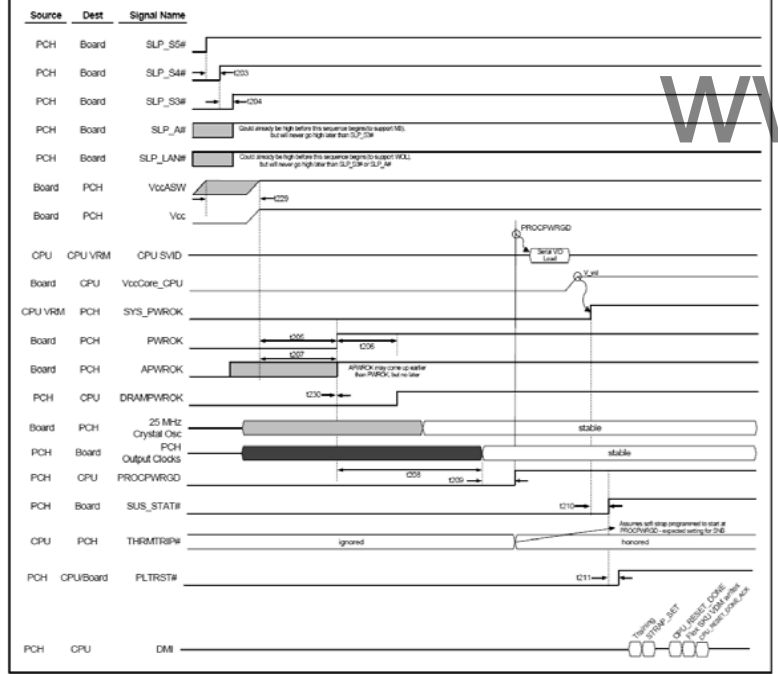
Deep Sleep Entry



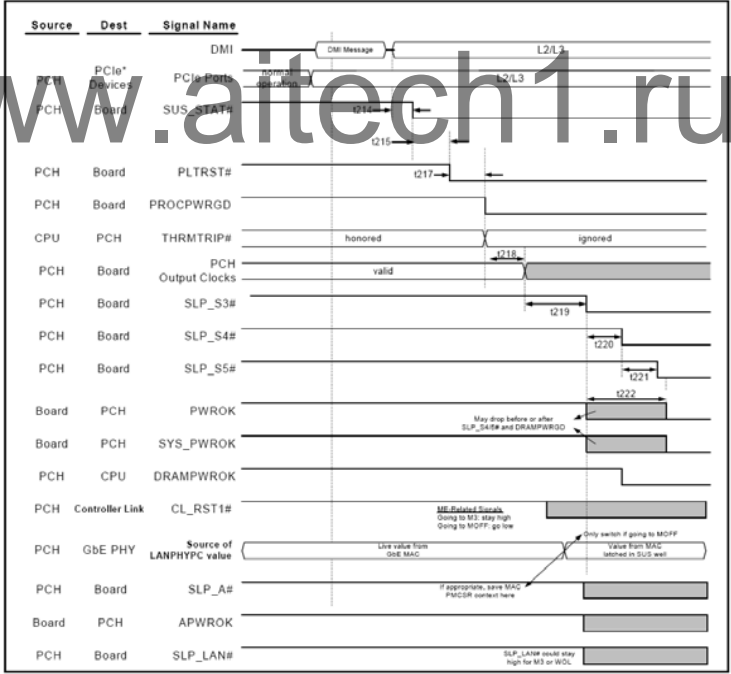
Deep Sleep Exit



S5 --> S0



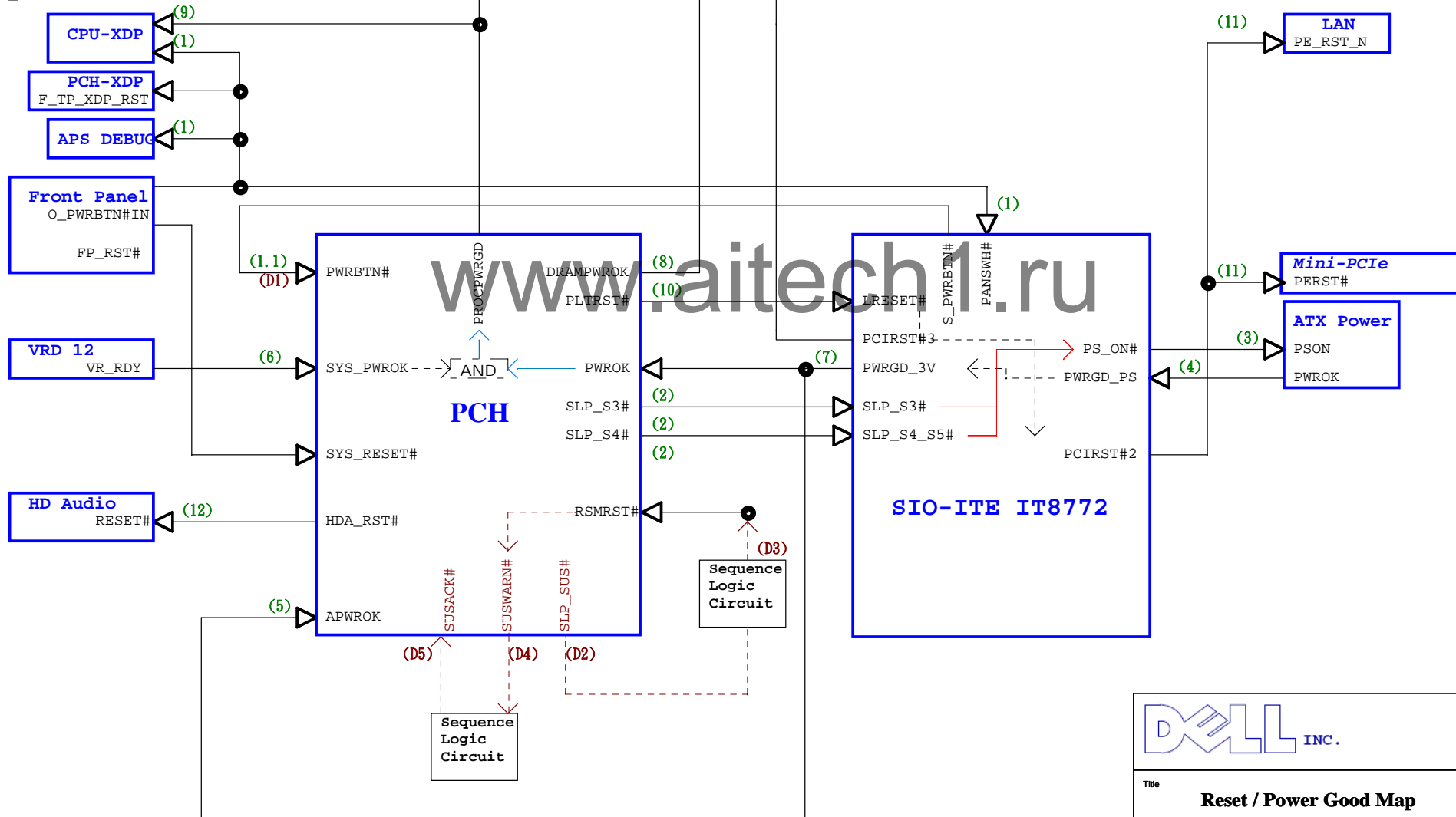
S0 --> S5



## RESET / Power Good MAP

### Sequence Signal Name:

- (1) O\_PWRBTN#IN
- (2) S\_SLP\_S4# S\_SLP\_S3# S\_SLP\_M#
- (3) O\_PSON#
- (4) B\_ATX\_PWROK
- (5) PCH\_MEPWROK
- (6) S\_PCH\_SYSPWROK P\_VR\_READY
- (7) PWRGD\_3V
- (8) H\_DRAMPWROK D3\_RESET#
- (9) H\_PWROK
- (10) S\_PLTRST# H RESET#\_R S\_PLTRST#\_R
- (11) X\_PLTRST\_PCIE\_SLOT# K\_PCIRST#\_SLOT
- (12) A\_Z\_RST#



## Deep Sleep Exit MAP

### Sequence Signal Name:

- (D1) O\_PWRBTN#IN
- (D2) S\_SLP\_SUS#
- (D3) S\_RSMRST#
- (D4) S\_SUSWARN#
- (D5) S\_SUS\_PWR\_ACK#



STRAPPING Table

CPU side

CFG[19:0]	Description	
[2]	PCI Express static x16 lane numbering reversal	1: normal <b>Default</b> 0: lane numbers reversed
[3]	PCI Express* Static x4 Lane Numbering Reversal	1 = Normal operation <b>Default</b> 0 = Lane numbers reversed
[6:5]	PCI Express Bifurcation	00: 1x8, 2x4 PCI Express 01: reserved 10: 2x8 PCI Express 11: 1x16 PCI Express <b>Default</b>

PCH

No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable

**DEFAULT**

Topblock Swap Mode

GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable

**DEFAULT**

Boot BIOS Destination Selection

GPIO51 (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI

SIO IT8772E/EX

PIN NAME	NET	Strapping description	
JP1 Pin23	JP1	1	EUP
		0	DSW <b>DEFAULT</b>
JP2 Pin57	O_RTS1#_R	1	Disable WDT to reset PWRGD <b>DEFAULT</b>
		0	Enable WDT to reset PWRGD
JP4 Pin61	O_DTR1#_R	1	Disable K8 power sequence function <b>DEFAULT</b>
		0	Enable K8 power sequence function
JP3 Pin59	O_TXD1_R	1	The default value of EC Index 63h/6Bh/73h is 80h <b>DEFAULT</b>
		0	The default value of EC Index 63h/6Bh/73h is 00h
JP8 Pin30	S_SLP_S3#	1	RSMRST# output detected by 3VSB <b>DEFAULT</b>
		0	RSMRST# output detected by SYS_3VSB

ME Disable (Flash override)

HDA_SDO	Description
High	ME Disable (Flash override): Enable
Low	ME Disable (Flash override): Disable

**DEFAULT**

TLS Confidentiality

SAAT3GP/ GPIO37	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality

**DEFAULT**

On-Die PLL Voltage Regulator

GPIO62/SUSCLK (IN-PU)	Description
High	Regulator is enabled.

**DEFAULT**

DMI Rx Termination

GPIO36 (IN-PD)	Description
Low	DMI Rx Termination Voltage



Title  
**GPIO/IRQ/IDSEL Table**

DWG NO  
**Goodyear**

Rev  
**A00**

GPIO	Type	Power Well	Default	IN-PU/PD	Mahobay B00		Function
					EX-PU/PD	Schematic net name	
GPIO[0]	VO	Core	GPI	-	10K pull-up to +3V	S_PECI_REQ#	Pull High only
GPIO[1]	VO	Core	GPI	20K IN-PU (Only on TACH1)	10K pull-up to +3V(dummy) 1K pull-down to GND	S_GPI_CHASSIS_ID0	GPI
GPIO[2]	VOD	Core	GPI	-	-	V_DDSF_D_HPD	GPI
GPIO[3]	VOD	Core	GPI	-	-	V_DDSF_C_HPD	GPI
GPIO[4]	VOD	Core	GPI	-	8.2K pull-up to +3V	V_GPI_VGA_CBL_DET#	GPI
GPIO[5]	VOD	Core	GPI	-	8.2K pull-up to +3V	PCIE_MINI_CPPE_DETECT#	GPI
GPIO[6]	VO	Core	GPI	20K IN-PU (Only on TACH2)	10K pull-up to +3V	S_GPI_PCH_HS_DET#	GPI
GPIO[7]	VO	Core	GPI	20K IN-PU (Only on TACH3)	10K pull-up to +3V(dummy) 220 pull-down to GND	S_GPI_SKU2	GPI
GPIO[8]	VO	Suspend	GPO	20K IN-PU	use as TP	S_TP_GP8	NC
GPIO[9]	VO	Suspend	Native	-	use as OC5# 8.2K pull-up to +3V_S5(dummy)	U_USB_OC_R_#5	Native
GPIO[10]	VO	Suspend	Native	-	10K pull-up to +3V_S5	U_USB_OC_R_#6	Pull High only
GPIO[11]	VO	Suspend	Native	-	10K pull-up to +3V_S5	X1_WAKE#_2	GPI
GPIO[12]	VO	Suspend	Native	-	10K pull-up to +3V_LAN (dummy) 4.7K pull-down to GND(dummy)	L_LAN_DISABLE#(H=Disable L=Enable)	GPO
GPIO[13]	VO	Suspend	GPI	-	10K pull-up to +3V_S5	X1_WAKE#_1	GPI
GPIO[14]	VO	Suspend	Native	-	8.2K pull-up to +3V_S5	GPD_WLOM	GPO
GPIO[15]	VO	Suspend	GPO	20K IN-PU	1K pull-up to +3V_S5	S_PCH_GP15	Pull High only
GPIO[16]	VO	Core	GPI	-	10K pull-up to +3V 10K pull-down to GND	H_SKTOCC_R_#	GPI
GPIO[17]	VO	Core	GPI	20K IN-PU (Only on TACH0)	10K pull-up to +3V(dummy) 1K pull-down to GND	S_GPI_CHASSIS_ID1	GPI
GPIO[19]	VO	Core	GPI	20K IN-PU	10K pull-up to +3V(dummy) 1K pull-down to GND(dummy)	S_SATA1GP	Native
GPIO[20]	VO	Core	Native	-	10K pull-up to +3V 10K pull-down to GND(dummy)	S_FLEXBAY_HDR_CBL_DET#	GPI
GPIO[21]	VO	Core	GPI	-	10K pull-up to +3V(dummy) 10K pull-down to GND	S_GPI_BRD_REV0	GPI
GPIO[22]	VO	Core	GPI	-	1K pull-up to +3V 4.7K pull-down to GND(dummy)	S_PCH_CONFIG_JUMPER	GPI
GPIO[23]	VO	Core	Native	20K IN-PU	10K pull-up to +3V(dummy)	L_DRQ1#	NC
GPIO[24]	VO	Suspend	GPO	-	100K pull-up to +3V_S5	H_SKTOCC#	GPI
GPIO[27]	VO	Deep Sleep	GPO	20K IN-PU	10K pull-up to +3V_DUAL 1K pull-down to GND(dummy)	S_GP27_PD	Pull High only
GPIO[28]	VO	Suspend	GPO	20K IN-PU	10K pull-up to +3V_S5 1K pull-down to GND(dummy)	S_PCH_GP28_PU	Pull High only
GPIO[29]	VO	Suspend	GPI	-	1K pull-up to +3V_S5(dummy)	S_SLP_LAN#	Native
GPIO[30]	VO	Deep Sleep	Native	-	10K pull-up to +3V_DUAL(dummy) 1K pull-down to GND(dummy)	S_SUSWARN#	Native
GPIO[31]	VO	Deep Sleep	GPI	TBD IN-PD	8.2K pull-up to +3V_DUAL	S_PSWD_CLR	GPI
GPIO[32]	VO	Core	GPO	-	10K pull-up to +3V(SKU) 220 pull-down to GND(SKU)	S_GPI_SKU0	GPI
GPIO[33]	VO	Core	GPO	-	use as TP	TPS38	NC
GPIO[34]	VO	Core	GPI	-	10K pull-up to +3V	PCH_GP034	Pull High only
GPIO[35]	VO	Core	GPO	-	10K pull-up to +3V(SKU) 220 pull-down to GND(SKU)	S_GPI_SKU1	GPI
GPIO[36]	VO	Core	GPI	20K IN-PD	use as TP	TPS27	NC

GPIO[37]	VO	Core	GPI	20K IN-PD	use as TP	TPS39	NC
GPIO[38]	VO	Core	GPI	-	10K pull-up to +3V(dummy) 10K pull-down to GND	S_GPI_CHASSIS_ID2	GPI
GPIO[39]	VO	Core	GPI	-	10K pull-up to +3V	A_FP_PRE#	GPI
GPIO[40]	VO	Suspend	Native	-	use as OC1#	U_USB_OC_R_#1	Native
GPIO[41]	VO	Suspend	Native	-	use as OC2#	U_USB_OC_R_#2	Native
GPIO[42]	VO	Suspend	Native	-	use as OC3#	U_USB_OC_R_#3	Native
GPIO[43]	VO	Suspend	Native	-	use as OC4# 8.2K pull-up to +3V(dummy)	U_USB_OC_R_#4	Native
GPIO[44]	VO	Suspend	Native	TBD IN-PD	10K pull-up to +3V_S5 10K pull-down to GND(dummy)	S_INTRUD_CBL_DET#	GPI
GPIO[45]	VO	Suspend	Native	-	10K pull-up to +3V_S5 10K pull-down to GND(dummy)	O_COM_SER2_DET#	GPI
GPIO[46]	VO	Suspend	Native	20K IN-PU	10K pull-up to +3V_S5(dummy) 1K pull-down to GND	S_GPI_BRD_REV1	GPI
GPIO[48]	VO	Core	GPI	-	10K pull-up to +3V	S_GPI048_PU	Pull High only
GPIO[49]	VO	Core	GPI	-	8.2K pull-up to +3V	TMN_SHIFT	Pull High only
GPIO[50]	VO	Core	Native	-	8.2K pull-up to +3V	K_REQ#1	Native
GPIO[51]	VO	Core	Native	20K IN-PU	1K pull-up to +3V(dummy) 1K pull-down to GND(dummy)	K_GNT#1	Native
GPIO[52]	VO	Core	Native	-	8.2K pull-up to +3V	K_REQ#2	Native
GPIO[53]	VO	Core	Native	20K IN-PU	1K pull-down to GND(dummy)	K_GNT#2	Native
GPIO[54]	VO	Core	Native	-	8.2K pull-up to +3V	K_REQ#3	Native
GPIO[55]	VO	Core	Native	20K IN-PU	4.7K pull-down to GND(dummy)	K_GNT#3	Native
GPIO[57]	VO	Suspend	GPI	-	10K pull-up to +3V_S5(dummy) 4.7K pull-down to GND	S_GPI057_PD	Pull Down only
GPIO[58]	VO	Suspend	Native	-	10K pull-up to +3V_S5	S_SMLINK1_CLK	Native
GPIO[59]	VO	Suspend	Native	-	use as OC0#	U_USB_OC_R_#0	Native
GPIO[60]	VO	Suspend	Native	-	2.2K pull-up to +3V_S5	GPIO_WIRELESS_DISABLE#	Pull High only
GPIO[61]	VO	Suspend	Native	-	8.2K pull-up to +3V_S5(dummy)	S_LPCPD#	NC
GPIO[62]	VO	Suspend	Native	-	use as susclk	S_SUSCLK	Native
GPIO[63]	VO	Suspend	Native	-	10K pull-up to +3V_S5	S_PCIAUX_GATE	GPO
GPIO[64]	VO	Core	Native	20K IN-PD	use as TP	S_TP_CLKOUTFLEX0	NC
GPIO[65]	VO	Core	Native	20K IN-PD	-	C_14M_SIO_R	Native
GPIO[66]	VO	Core	Native	20K IN-PD	use as TP	S_TP_CLKOUTFLEX0	NC
GPIO[67]	VO	Core	Native	20K IN-PD	-	C_14M_TPM_R	Native
GPIO[68]	VO	Core	GPI	20K IN-PU (Only on TACH4)	10K pull-up to +3V(dummy) 220 pull-down to GND	S_GPI_BRD_REV2	GPI
GPIO[69]	VO	Core	GPI	20K IN-PU (Only on TACH5)	10K pull-up to +3V	O_PRT_DET#	Pull High only
GPIO[70]	VO	Core	GPI	20K IN-PU (Only on TACH6)	8.2K pull-up to +3V	S_FF_CHAS_DET#	GPI
GPIO[71]	VO	Core	GPI	20K IN-PU (Only on TACH7)	10K pull-up to +3V	-	Pull High only
GPIO[72]	VO	Suspend	Native (Mobile Only)	20K IN-PU	10K pull-up to +3V_S5	S_PCH_GP72_PU	Pull High only
GPIO[74]	VO	Suspend	Native	-	10K pull-up to +3V_S5	S_MFG_MODE_OR	GPI
GPIO[75]	VO	Suspend	Native	-	10K pull-up to +3V_S5	S_SMLINK1_DATA	Native

GPIO	PIN NAME	Power well	Buffer Type	EX-PU/PD	Signal Name
OP000	(DIAO_LED3#) OP000	VTR	IO	NA	O_DIAO_LED3#
OP001	(DIAO_LED1#) OP001	VTR	IO	NA	O_DIAO_LED1#
OP002	(DIAO_LED2#) OP002	VTR	IO	NA	O_DIAO_LED2#
OP003	(DIAO_LED4#) OP003	VTR	IO	NA	O_DIAO_LED4#
OP004	OP004	VTR	IO	NA	NC
OP005	(H_CPU_RST#) GP005 / PECIAL_REQUEST#	VTR	IO/OD	10k pull-up to +3V	O_PECIAL_REQ#
OP006	YELLOW# / OP006	VTR	ODIO	NA	O_YELLOW#
OP007	GREEN# / OP007	VTR	ODIO	NA	O_GREEN#
OP010	SMBDATA2 / OP010	VTR	IODIO	8.2k pull-up to +3V_DUAL(dummy)	S_SMLINK1_DATA_R
OP011	SMBCLK2 / OP011	VTR	IODIO	8.2k pull-up to +3V_DUAL (dummy)	S_SMLINK1_CLK_R
OP012	OP012	VTR	IO	8.2k pull-up to +3V_DUAL	SP1_DI
OP013	OP013	VTR	IO	NA	NC
OP014	(TMN_SHIFT) OP014	VTR	IO	8.2k pull-up to +3V	TMN_SHIFT
OP015	PWRBTN# / OP015	VTR	IO	1k pull-up to +3V_DUAL	O_PWRBTNN
OP016	PROCHOT_IN# / PROCHOT_OUT# / OP016	VTR	IODIOD	510hm pull-up to +1P05V_VCCIO	H_PROCHOT#
OP017	TACH1 / OP017	VTR	IO	1k pull-up to +3V	O_SEN_CUFAN
OP020	TACH2 / OP020	VTR	IO	1k pull-up to +3V	O_SEN_CHAFAN
OP021	TACH3 / OP021	VTR	IO	NA	NC
OP022	PWM1 / OP022	VTR	ODIO	4.7k pull-up to +3V	O_CPUFAN_PWM
OP023	PWM2 / OP023	VTR	ODIO	4.7k pull-up to +3V	O_CHAFAN_PWM
OP024	PWM3 / OP024	VTR	ODIO	NA	NC
OP025	(FP_CBL_DET#) OP025	VTR	IO	8.2k pull-up to +3V_S5	O_FP_CBL_DET#
OP026	PC_L_RST_SYS# / OP026	VTR	ODIO	NA	X1_FLTRST_FCE_SLOT#
OP027	PC_L_RST_SLOT# / OP027	VTR	ODIO	NA	H_RESET#
OP030	PS_ON# / OP030	VTR	ODIO	4.7k pull-up to +5VSB	O_PSON#
OP031	(FC_SPKR_DET) OP031	VTR	IO	8.2k pull-up to +3V_DUAL	O_AUD_PCSPKR_DET#
OP032	OP032	VTR	IO	NA	NC
OP033	PWR_ODD_3V / OP033	VTR	ODIO	NA	PWR_ODD_3V
OP034	RSMRST# / OP034	VTR	ODIO	10k pull-down to GND	O_RSMRST#
OP035	OP035	VTR	IO	8.2k pull-up to +3V_DUAL	O_BC_CLK
OP036	OP036 / SMB_CLK1	VTR	IODIO	8.2k pull-up to +3V_DUAL (dummy)	S_SMBCLK_PCL_R
OP040	OP040 / SMB_DAT1	VTR	IODIO	8.2k pull-up to +3V_DUAL (dummy)	S_SMBDATA_PCL_R
OP041	OP041 / IO_FME#	VTR	IODIO	10k pull-up to +3V_S5	O_IO_FME#
OP042	GP042 / DRVDE0	VTR	IODIO	100k pull-up to +3V_DUAL(dummy)	T_ESATA_DET#
OP043	DCD1# / GP043 / MCDAT	VTR	IO/IO	NA	O_DCD1#_R
OP044	DSR1# / GP044 / MCCLK	VTR	IO/IO	NA	O_DSR1#_R
OP045	RxD1 / GP045	VTR	IO	NA	O_RxD1_R
OP046	RTS1# / GP046	VTR	ODIO	NA	O_RTS1#_R
OP047	(SV_PRSNT) OP047 / TXD1	VTR	ODIO	NA	O_TXD1_R
OP050	CTS1# / GP050	VTR	IO	NA	O_CTS1#_R
OP051	DTR1# / TEST_EN / GP051	VTR	ODIO	8.2k pull-up to +3V_DUAL(dummy) 20k pull-down to GND	O_DTR1#_R
OP052	R1# / OP052	VTR	IO	NA	O_R1#_R
OP053	OP053 / DCD2#	VTR	IO	2.2k pull-up to +3V	O_DCD2#_R
OP054	OP054 / DSR2#	VTR	IO	2.2k pull-up to +3V	O_DSR2#_R
OP055	OP055 / RxD2	VTR	IO	2.2k pull-up to +3V	O_RxD2_R
OP056	(PWR2_PRSNT) OP056 / RTS2#	VTR	IODIO	30k pull-up to +3V	O_RTS2#_R
OP057	(MB_REG_FQ) GP057 / TXD2	VTR	IODIO	30k pull-up to +3V	O_TXD2_R
OP060	OP060 / CTS2#	VTR	IO	2.2k pull-up to +3V	O_CTS2#_R
OP061	(MEM_REG_FQ) GP061 / DTR2#	VTR	IODIO	30k pull-up to +3V	O_DTR2#_R
OP062	OP062 / R1#	VTR	IO	2.2k pull-up to +3V	O_R1#_R
OP063	GP063 / KBORST#	VTR	IODIO	10k pull-up to +3V	O_KB_RST#
OP064	OP064 / A20M	VTR	IODIO	10k pull-up to +3V	O_A20
OP065	SLP_S3# / GP065	VTR	IO	NA	S_SLP_S3#
OP066	SLP_S4_S5# / GP066	VTR	IO	NA	S_SLP_S4#
OP067	PWROD_P5 / OP067	VTR	IO	1k pull-up to +5V	B_ATT_PVR0K
OP070	SPEAKER [DIAO_EN#] / OP070	VTR	ODIO	8.2k pull-up to +3V_DUAL(dummy) 8.25k pull-down to GND	O_SPEAKER
OP071	(SLP_M#) OP071 / IO_SMI#	VTR	IODIO	NA	S_SLP_M#
OP072	PECL1 / LVSMB_CLK1 / GP072	VTR	PECL1/ODIODIO	1k pull-up to +1P05V_VCCIO (dummy)	H_PEC1_R
OP073	PECL1_READY / LVSMB_DAT1 / GP073	VTR	PECL1/IODIODIO	1k pull-up to +1P05V_VCCIO	O_OP73_PU



## GPIO Table

# DDR3 CH-A

15,16 D3\_DQ\_A[63..0] <<>

D3\_MAA[15..0] 15,16

ECC

D3\_CKE\_A0 15  
D3\_CKE\_A1 15  
D3\_CKE\_A2 16  
D3\_CKE\_A3 16

D3\_SCs\_A#0 15  
D3\_SCs\_A#1 15  
D3\_SCs\_A#2 16  
D3\_SCs\_A#3 16

D3\_MA\_CLK#0 15  
D3\_MA\_CLK#1 15  
D3\_MA\_CLK#2 16  
D3\_MA\_CLK#3 16

D3\_RAS# 15,16  
D3\_WE# 15,16

D3\_CAS# 15,16  
D3\_SM\_DRAMRST#  
D3\_RESET# 15,16,17,18

BIT SWIZZLE TABLE

DDR0_DQ[8]	AH40	DQ 9
DDR0_DQ[9]	AH39	DQ 13
DDR0_DQ[13]	AH38	DQ 8
DDR0_DQ[16]	AM40	DQ 17
DDR0_DQ[17]	AM39	DQ 21
DDR0_DQ[21]	AM38	DQ 16
DDR0_DQ[24]	AV37	DQ 25
DDR0_DQ[25]	AW37	DQ 29
DDR0_DQ[29]	AU37	DQ 24
DDR0_DQ[32]	AY6	DQ 33
DDR0_DQ[33]	AU6	DQ 37
DDR0_DQ[37]	AV6	DQ 32
DDR0_DQ[40]	AR1	DQ 41
DDR0_DQ[41]	AR4	DQ 45
DDR0_DQ[45]	AR3	DQ 40
DDR0_DQ[48]	AL1	DQ 49
DDR0_DQ[49]	AL4	DQ 53
DDR0_DQ[53]	AL3	DQ 48
DDR0_DQ[56]	AG1	DQ 57
DDR0_DQ[57]	AG4	DQ 61
DDR0_DQ[61]	AG3	DQ 56
DDR0_DQ[64]	AW33	DQ 65
DDR0_DQ[65]	AV33	DQ 69
DDR0_DQ[69]	AU33	DQ 64

Bit Swap for layout

ECC

ECC

1 OF 10

PE115027-4041-0DF



Title  
**CPU-1: DDR3\_CHA**

DWG NO  
**Goodyear**  
Rev  
**X02**

Date: 星期三, 二月 20, 2013 Sheet 9 of 57

# DDR3 CH-B

17,18 D3\_DQ\_B[63..0]

UH1B

D3 DQ B0	AE34	SB DQ[0]
D3 DQ B1	AE35	SB DQ[1]
D3 DQ B2	AG35	SB DQ[2]
D3 DQ B3	AH35	SB DQ[3]
D3 DQ B4	AD35	SB DQ[4]
D3 DQ B5	AD35	SB DQ[5]
D3 DQ B6	AG34	SB DQ[6]
D3 DQ B7	AH34	SB DQ[7]
D3 DQ B8	AL34	SB DQ[8]
D3 DQ B9	AL35	SB DQ[9]
D3 DQ B10	AK31	SB DQ[10]
D3 DQ B11	AL31	SB DQ[11]
D3 DQ B12	AK34	SB DQ[12]
D3 DQ B13	AK35	SB DQ[13]
D3 DQ B14	AK32	SB DQ[14]
D3 DQ B15	AL32	SB DQ[15]
D3 DQ B17	AP34	SB DQ[16]
D3 DQ B21	AP34	SB DQ[17]
D3 DQ B19	AN31	SB DQ[18]
D3 DQ B23	AP31	SB DQ[19]
D3 DQ B20	AN35	SB DQ[20]
D3 DQ B16	AP35	SB DQ[21]
D3 DQ B18	AN32	SB DQ[22]
D3 DQ B22	AP32	SB DQ[23]
D3 DQ B25	AM29	SB DQ[24]
D3 DQ B28	AM28	SB DQ[25]
D3 DQ B27	AR29	SB DQ[26]
D3 DQ B30	AR28	SB DQ[27]
D3 DQ B24	AL29	SB DQ[28]
D3 DQ B29	AL28	SB DQ[29]
D3 DQ B26	AP29	SB DQ[30]
D3 DQ B31	AP28	SB DQ[31]
D3 DQ B32	AR12	SB DQ[32]
D3 DQ B33	AP12	SB DQ[33]
D3 DQ B34	AL13	SB DQ[34]
D3 DQ B35	AL12	SB DQ[35]
D3 DQ B36	AR13	SB DQ[36]
D3 DQ B37	AP13	SB DQ[37]
D3 DQ B38	AM13	SB DQ[38]
D3 DQ B39	AM12	SB DQ[39]
D3 DQ B45	AR9	SB DQ[40]
D3 DQ B41	AP9	SB DQ[41]
D3 DQ B47	AR6	SB DQ[42]
D3 DQ B43	AP6	SB DQ[43]
D3 DQ B44	AR10	SB DQ[44]
D3 DQ B40	AP10	SB DQ[45]
D3 DQ B46	AR7	SB DQ[46]
D3 DQ B42	AP7	SB DQ[47]
D3 DQ B52	AM9	SB DQ[48]
D3 DQ B53	AL9	SB DQ[49]
D3 DQ B50	AL6	SB DQ[50]
D3 DQ B55	AL7	SB DQ[51]
D3 DQ B48	AM10	SB DQ[52]
D3 DQ B49	AL10	SB DQ[53]
D3 DQ B54	AM6	SB DQ[54]
D3 DQ B51	AM7	SB DQ[55]
D3 DQ B61	AH6	SB DQ[56]
D3 DQ B60	AH7	SB DQ[57]
D3 DQ B59	AE6	SB DQ[58]
D3 DQ B63	AE7	SB DQ[59]
D3 DQ B56	AJ6	SB DQ[60]
D3 DQ B57	AJ7	SB DQ[61]
D3 DQ B58	AF6	SB DQ[62]
D3 DQ B62	AF7	SB DQ[63]
17,18 D3_DQS_B0	AF35	SB DQS[0]
17,18 D3_DQS_B1	AL33	SB DQS[1]
17,18 D3_DQS_B2	AP33	SB DQS[2]
17,18 D3_DQS_B3	AN28	SB DQS[3]
17,18 D3_DQS_B4	AN12	SB DQS[4]
17,18 D3_DQS_B5	AL8	SB DQS[5]
17,18 D3_DQS_B6	AL8	SB DQS[6]
17,18 D3_DQS_B7	AG7	SB DQS[7]
17,18 D3_DQS_B8	AN25	SB DQS[8]
17,18 D3_DQS_B#0	AF34	SB DQS[9]
17,18 D3_DQS_B#1	AK33	SB DQS[10]
17,18 D3_DQS_B#2	AN33	SB DQS[11]
17,18 D3_DQS_B#3	AN29	SB DQS[12]
17,18 D3_DQS_B#4	AN13	SB DQS[13]
17,18 D3_DQS_B#5	AR8	SB DQS[14]
17,18 D3_DQS_B#6	AM8	SB DQS[15]
17,18 D3_DQS_B#7	AG6	SB DQS[16]
17,18 D3_DQS_B#8	AN26	SB DQS[17]

SB MA[0]	AL19	D3 MAB0
SB MA[1]	AK23	D3 MAB1
SB MA[2]	AM22	D3 MAB2
SB MA[3]	AM23	D3 MAB3
SB MA[4]	AP23	D3 MAB4
SB MA[5]	AL23	D3 MAB5
SB MA[6]	AY24	D3 MAB6
SB MA[7]	AV25	D3 MAB7
SB MA[8]	AU26	D3 MAB8
SB MA[9]	AW25	D3 MAB9
SB MA[10]	AP18	D3 MAB10
SB MA[11]	AY25	D3 MAB11
SB MA[12]	AV26	D3 MAB12
SB MA[13]	AR15	D3 MAB13
SB MA[14]	AV27	D3 MAB14
SB MA[15]	AY28	D3 MAB15

D3\_MAB[15..0] 17,18

SB_ODT[0]	AM17	D3_ODT_B0 17
SB_ODT[1]	AL16	D3_ODT_B1 17
SB_ODT[2]	AM16	D3_ODT_B2 18
SB_ODT[3]	AK15	D3_ODT_B3 18

SB_ECC_CB[0]	AM26	D3_SB_ECC_CB4 17,18
SB_ECC_CB[1]	AM25	D3_SB_ECC_CB5 17,18
SB_ECC_CB[2]	AP25	D3_SB_ECC_CB6 17,18
SB_ECC_CB[3]	AL26	D3_SB_ECC_CB7 17,18
SB_ECC_CB[4]	AL25	D3_SB_ECC_CB8 17,18
SB_ECC_CB[5]	AR26	D3_SB_ECC_CB1 17,18
SB_ECC_CB[6]	AR25	D3_SB_ECC_CB2 17,18
SB_ECC_CB[7]	AR25	D3_SB_ECC_CB3 17,18

ECC

D3\_BAB[2..0] 17,18

SB_BS[0]	AK17	D3_BAB0
SB_BS[1]	AL18	D3_BAB1
SB_BS[2]	AW28	D3_BAB2

SB_CKE[0]	AW29	D3_CKE_B0 17
SB_CKE[1]	AY29	D3_CKE_B1 17
SB_CKE[2]	AU28	D3_CKE_B2 18
SB_CKE[3]	AU29	D3_CKE_B3 18

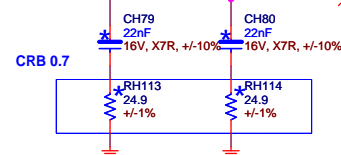
SB_CS[0]	AP17	D3_SCB_B#0 17
SB_CS[1]	AN15	D3_SCB_B#1 17
SB_CS[2]	AN17	D3_SCB_B#2 18
SB_CS[3]	AL15	D3_SCB_B#3 18

SB_CLK[0]	AN20	D3_MB_CLK0 17
SB_CLK[1]	AM21	D3_MB_CLK#0 17
SB_CLK[2]	AP22	D3_MB_CLK#1 17
SB_CLK[3]	AP21	D3_MB_CLK#2 18

SB_CLK[2]	AN20	D3_MB_CLK#2 18
SB_CLK[2]	AN21	D3_MB_CLK#3 18
SB_CLK[3]	AP19	D3_MB_CLK#3 18
SB_CLK[3]	AP20	D3_MB_CLK#3 18

SB_CAS#	AP16	D3_CASB# 17,18
RSVD_49	AL20	D3_CASB# 17,18
SB_RAS#	AM18	D3_RASB# 17,18
SB_WE#	AK16	D3_WEB# 17,18

SA_DIMM_VREFDQ	AB39	H_CPU_DIMM_VREF_A 15
SB_DIMM_VREFDQ	AB40	H_CPU_DIMM_VREF_B 17



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PE115027-4041-0DF

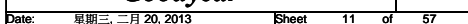


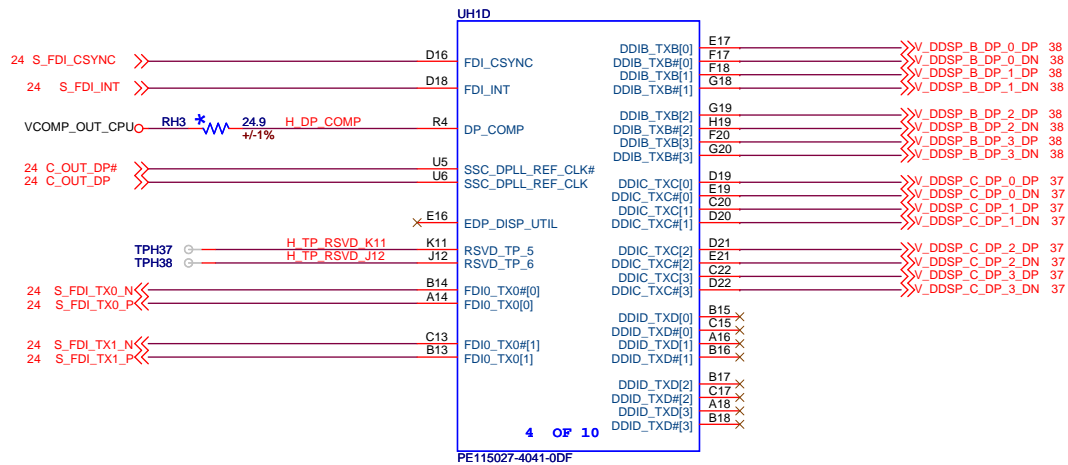
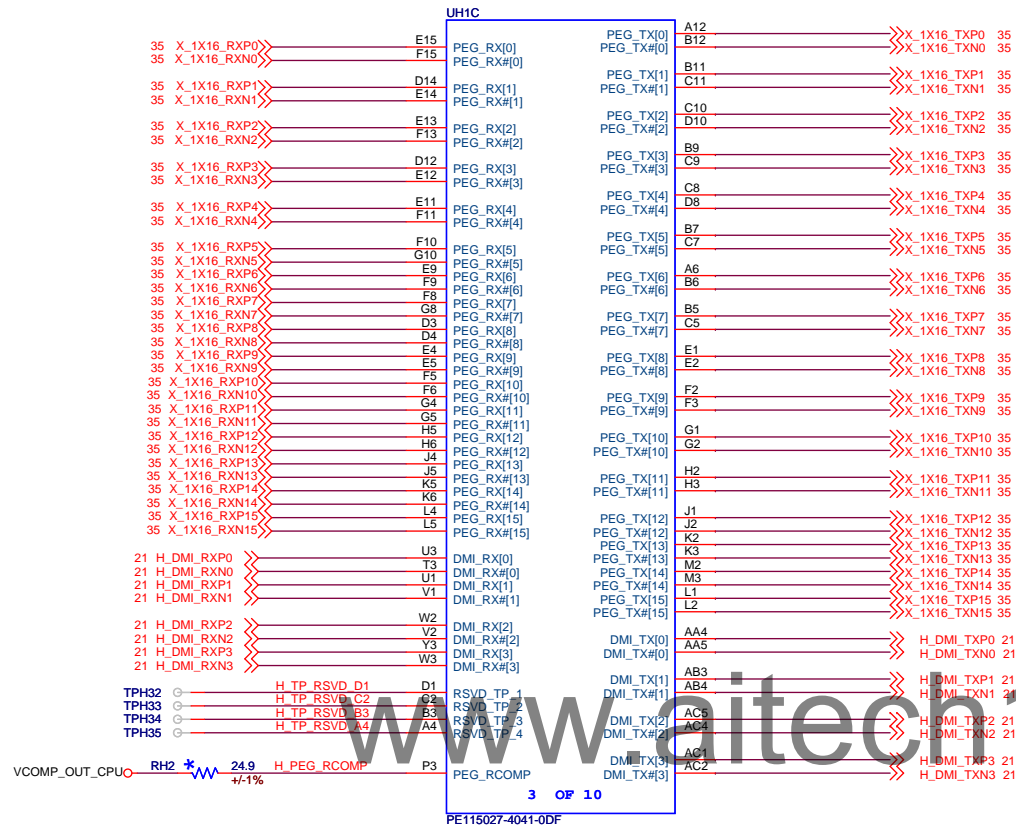
Title CPU-2: DDR3\_CHB

DWG NO Goodyear Rev A00

Date: 星期三, 二月 20, 2013 Sheet 10 of 57







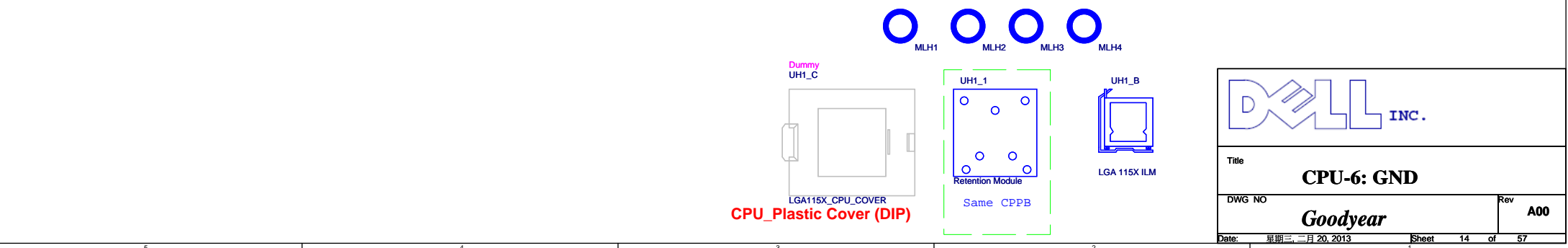
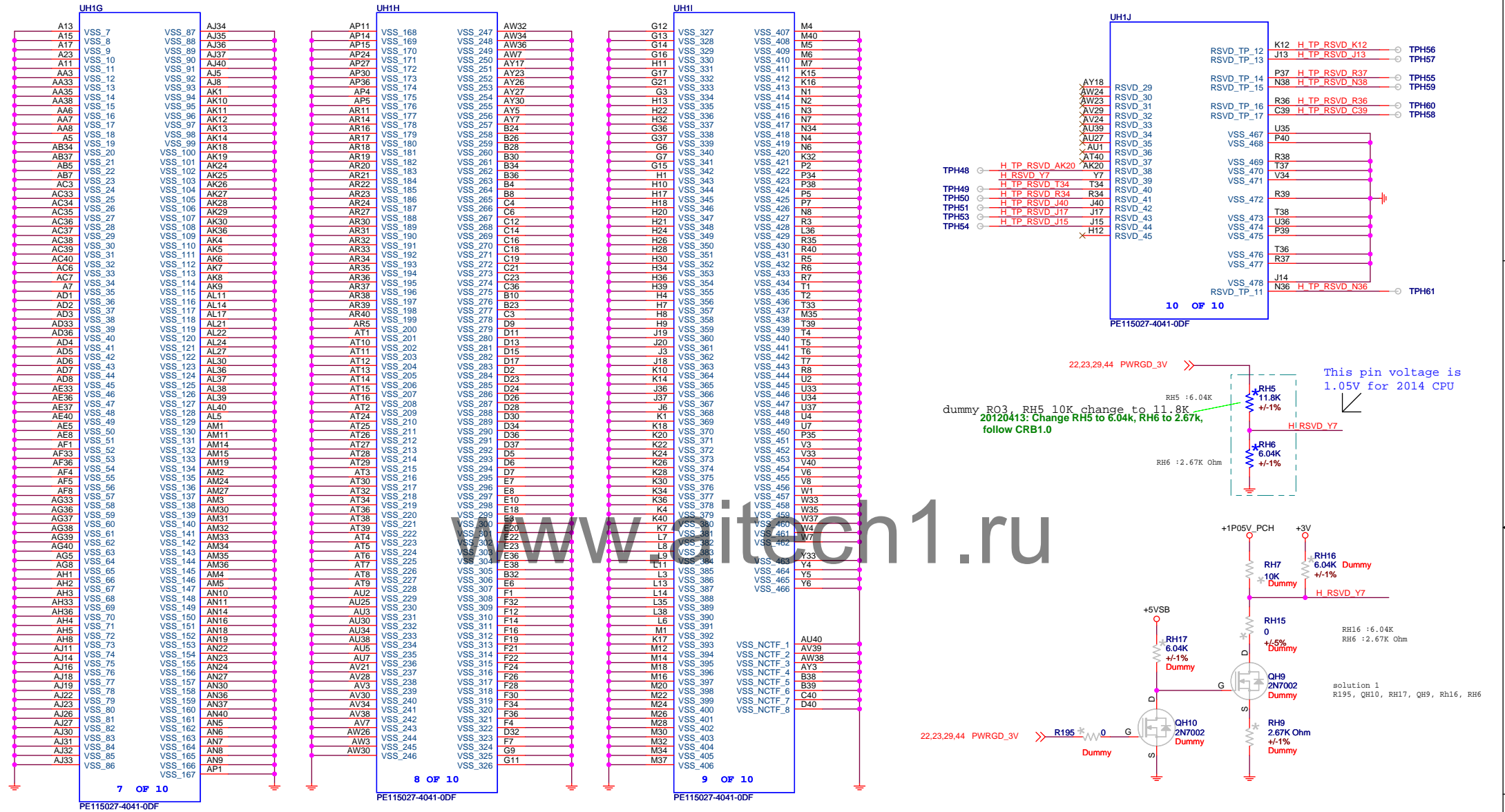
Display Port

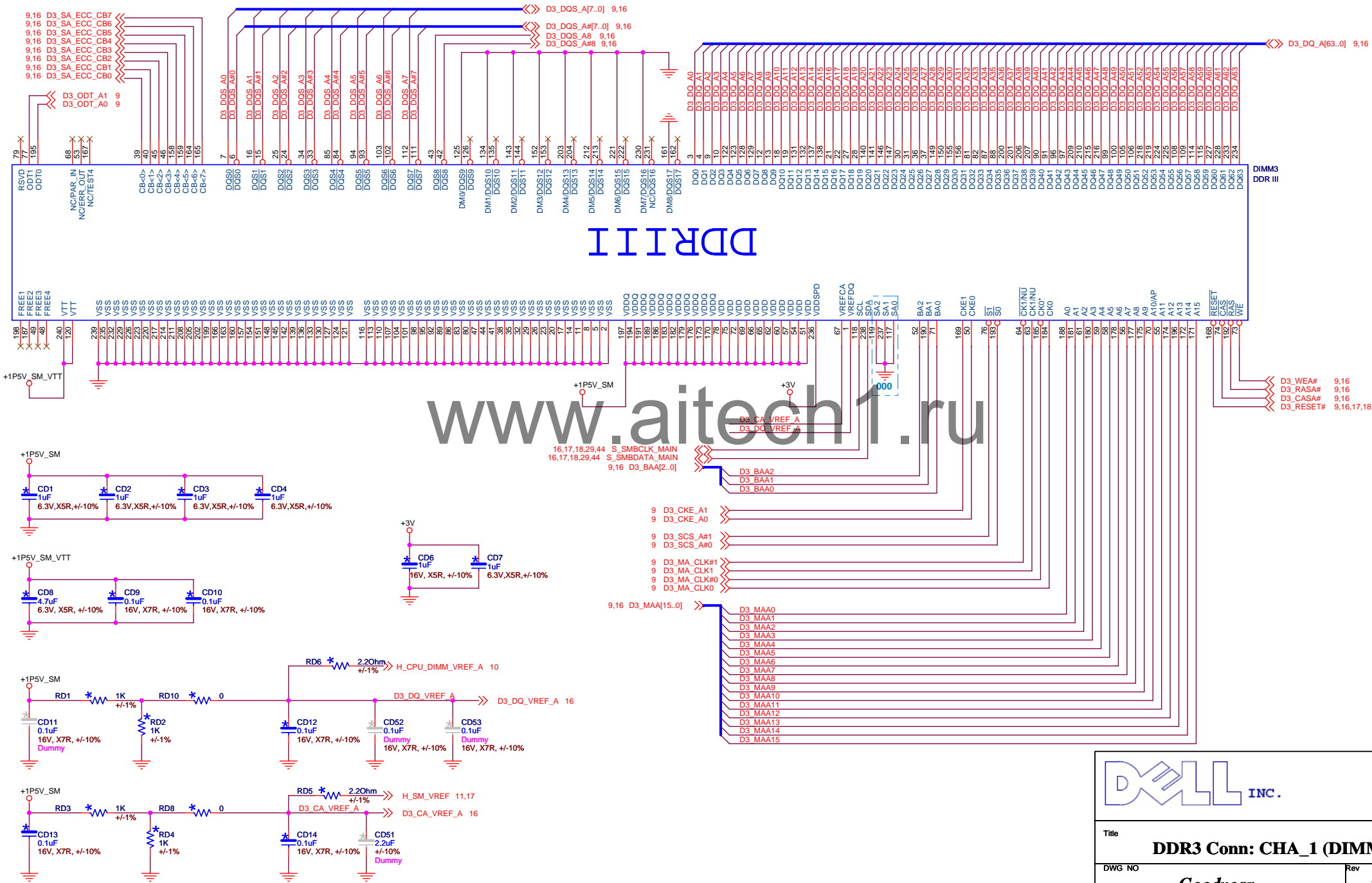
HDMI



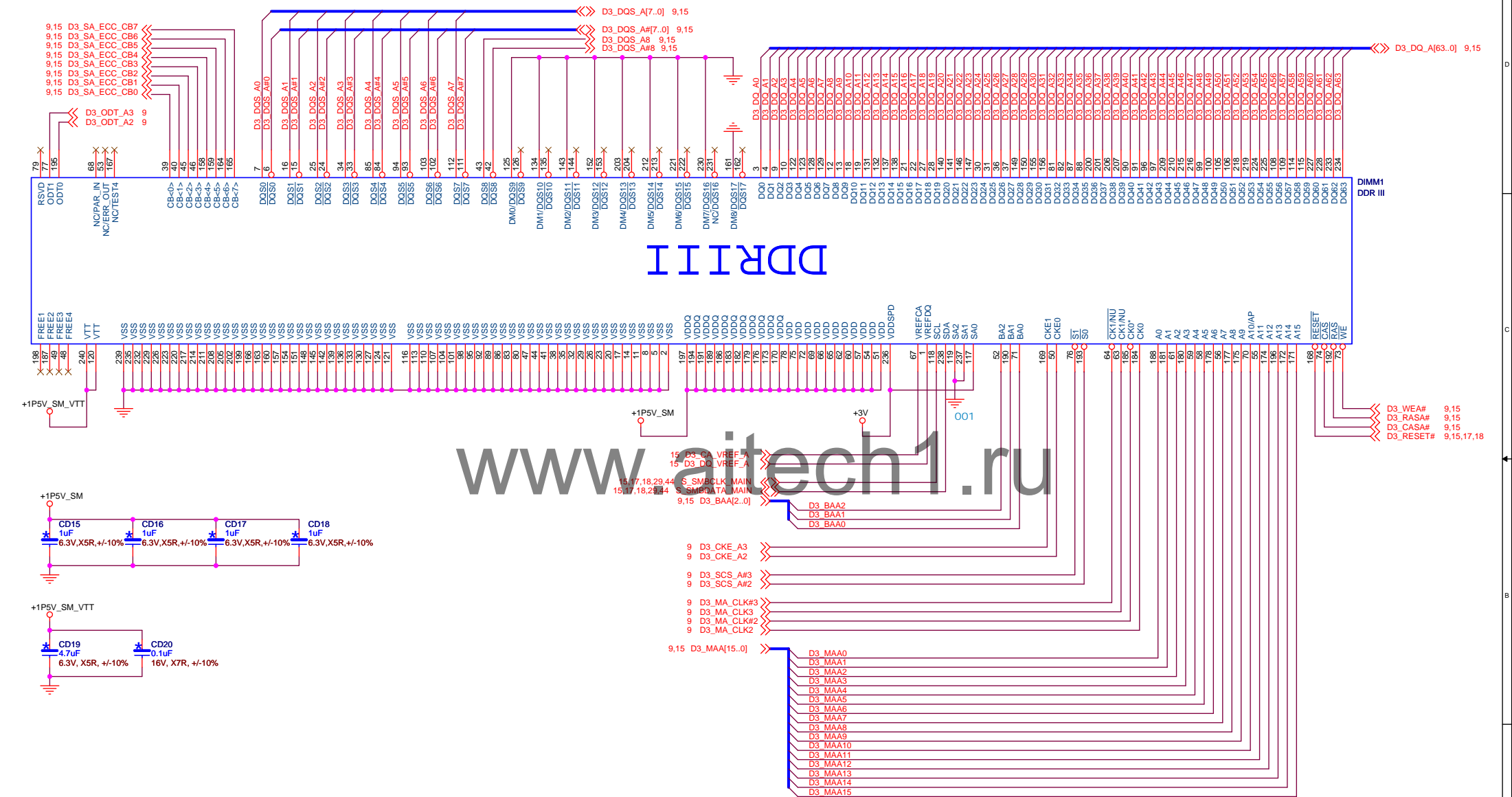






**DDR3 Conn: CHA\_1 (DIMM3)**

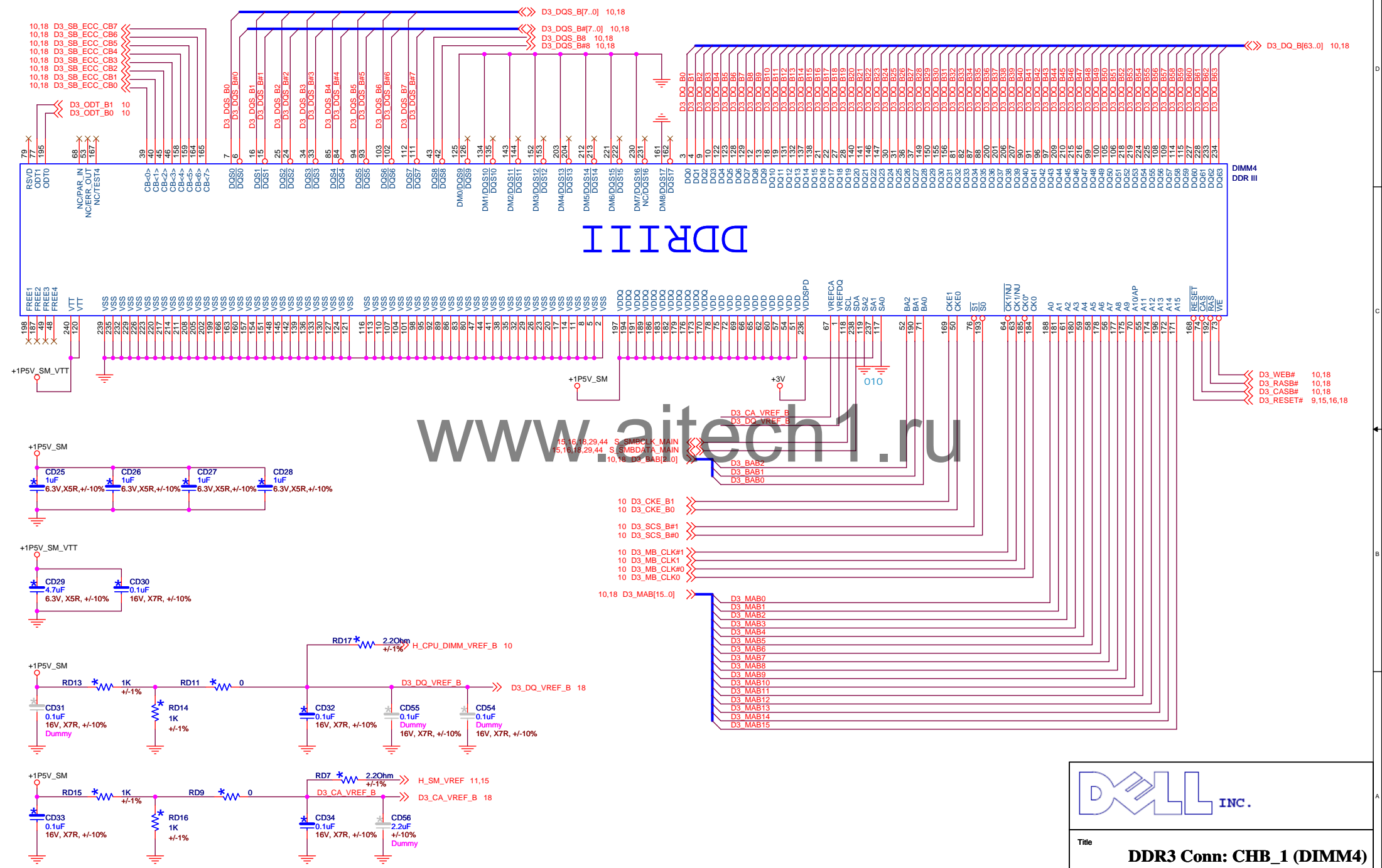
DWG NO	Rev
<i>Cadbury</i>	A00


**DDR3 Conn: CHA\_2 (DIMM1)**

DWG NO	Rev
	A00

**Goodyear**

400



 **INC.**

Title

**DDR3 Conn: CHB\_1 (DIMM4)**

DWG NO

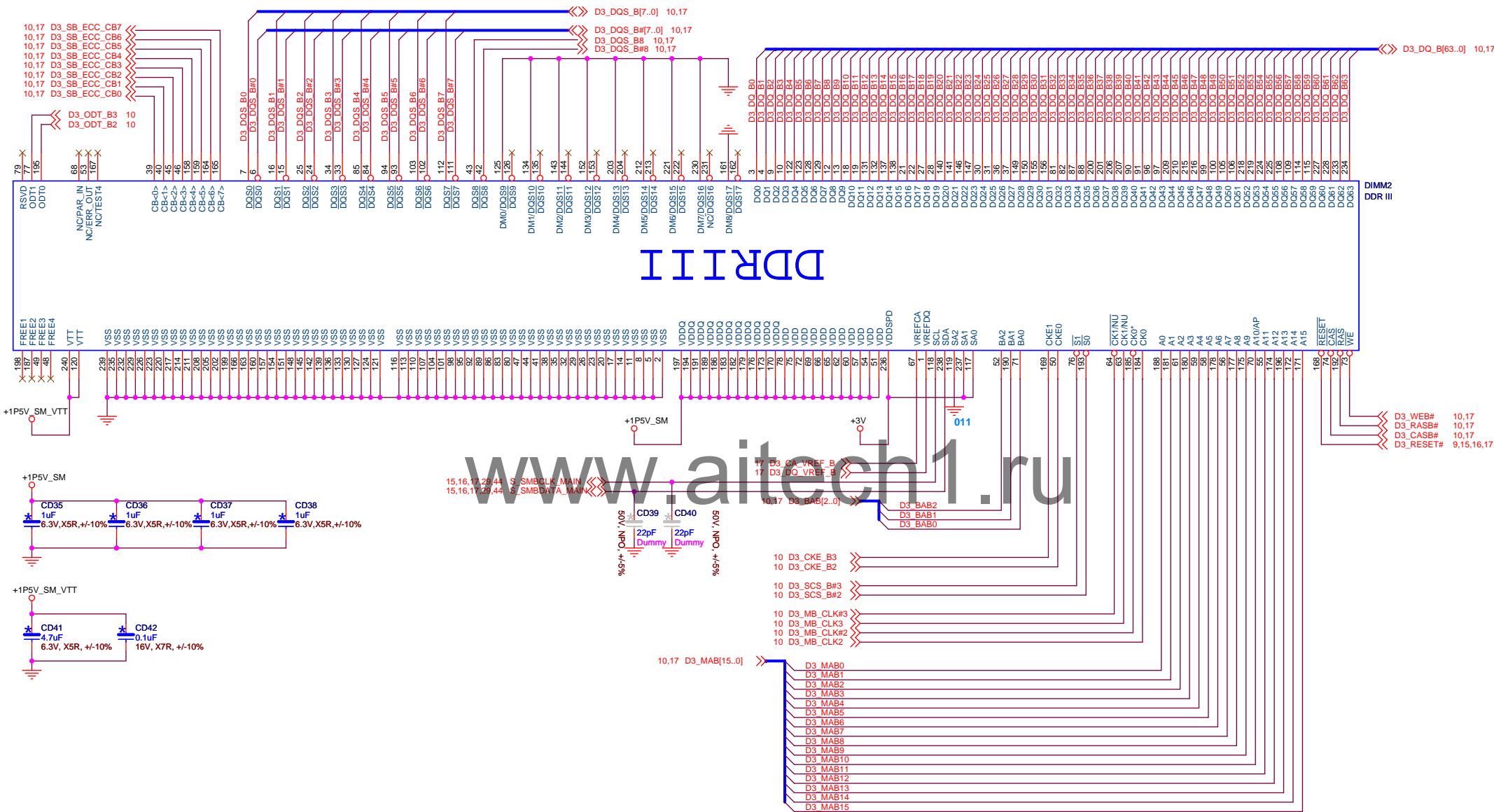
**Goodyear**

Rev

**A00**


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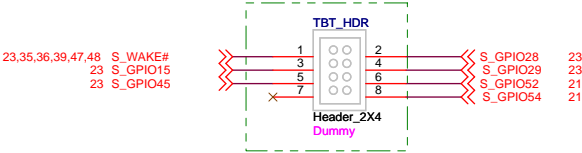
**DDR3 Conn: CHB\_2 (DIMM2)**

DWG NO	Rev
	A00

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Title <b>Label</b>		
DWG NO <b>Goodyear</b>		Rev <b>A00</b>
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20120626: Add TBT\_HDR  
20120703: TBT\_HDR compoment  
REMARK cahnge to Remark

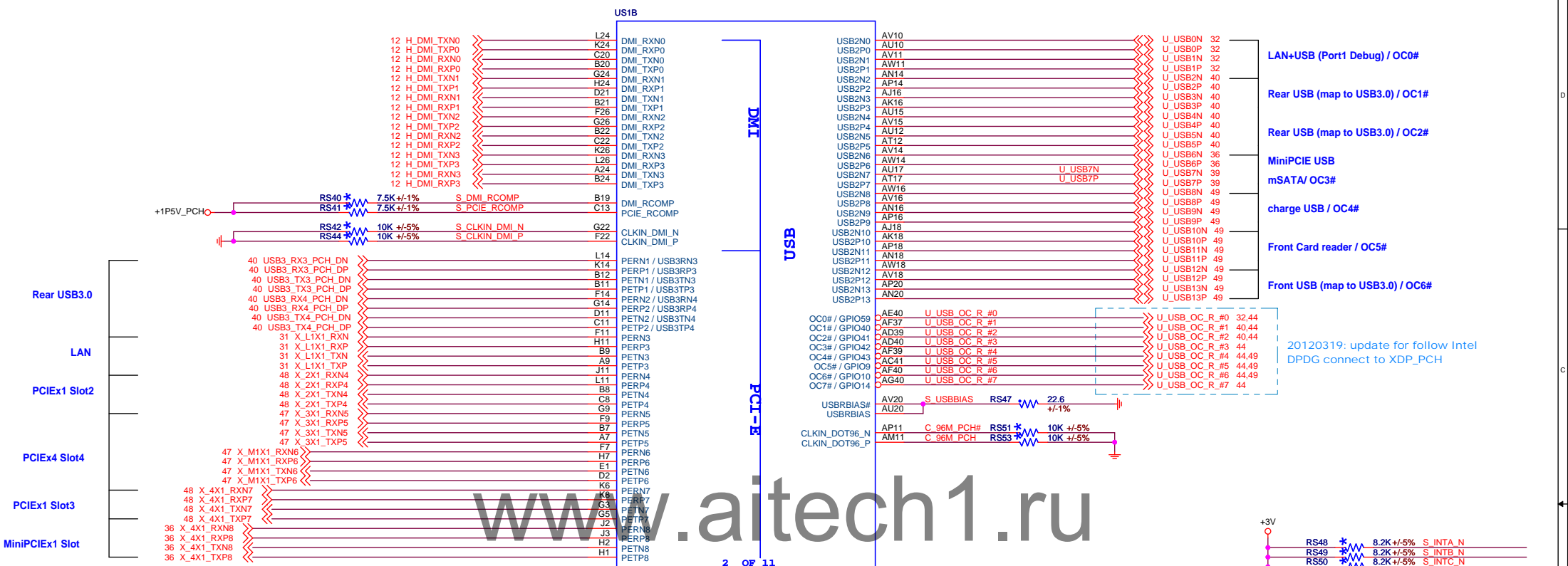


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Title			TBD		
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			Rev A00		






- LAN+USB (Port1 Debug) / OC0#
- Rear USB (map to USB3.0) / OC1#
- Rear USB (map to USB3.0) / OC2#
- MiniPCIe USB
- mSATA/ OC3#
- charge USB / OC4#
- Front Card reader / OC5#
- Front USB (map to USB3.0) / OC6#

20120319: update for follow Intel  
DPDG connect to XDP\_PCH

- RS48 8.2K +/-5% S\_INTA\_N
- RS49 8.2K +/-5% S\_INTB\_N
- RS50 8.2K +/-5% S\_INTC\_N
- RS52 8.2K +/-5% S\_INTD\_N
- RS54 8.2K +/-5% F\_USB\_DETECT1
- RS55 8.2K +/-5% PCIE\_MINI\_CPPE\_DETECT#
- RS56 8.2K +/-5% PCIE\_MINI\_CPUSB\_DETECT#
- RS64 8.2K +/-5% V\_DDSP\_C\_HPD\_C
- RS43 8.2K +/-5% U\_USB\_OC\_R\_#3
- RS57 8.2K +/-5% U\_USB\_OC\_R\_#4
- RS45 8.2K +/-5% U\_USB\_OC\_R\_#6
- RS46 8.2K +/-5% U\_USB\_OC\_R\_#7
- RS149 10K +/-5% S\_GPIO52
- RS173 10K +/-5% S\_GPIO54
- RS174 10K +/-5% S\_GPIO50

**INC.**

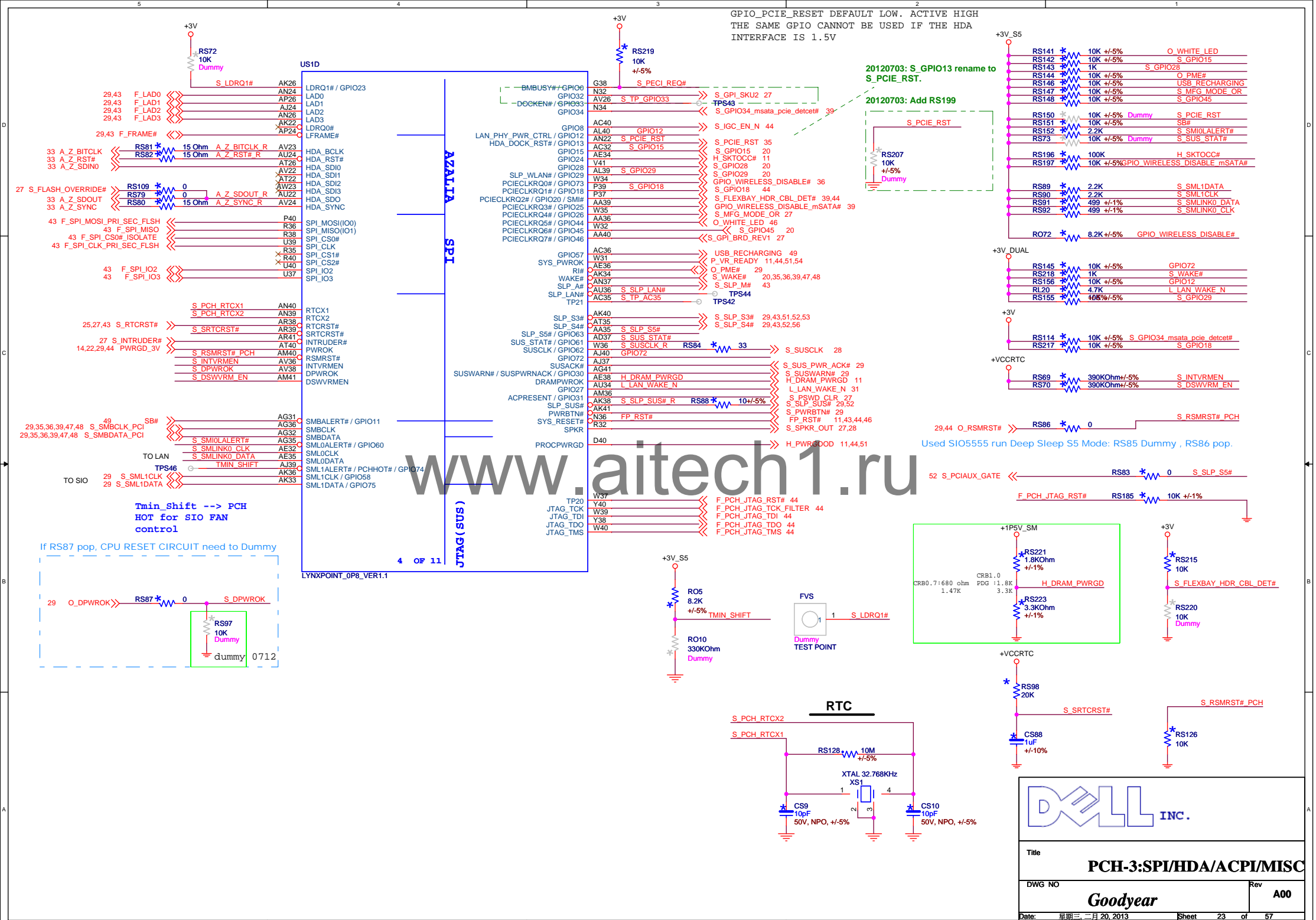
**Title**  
**PCH-1: DMI/USB/PCIe**

**DWG NO**  
**Goodyear**

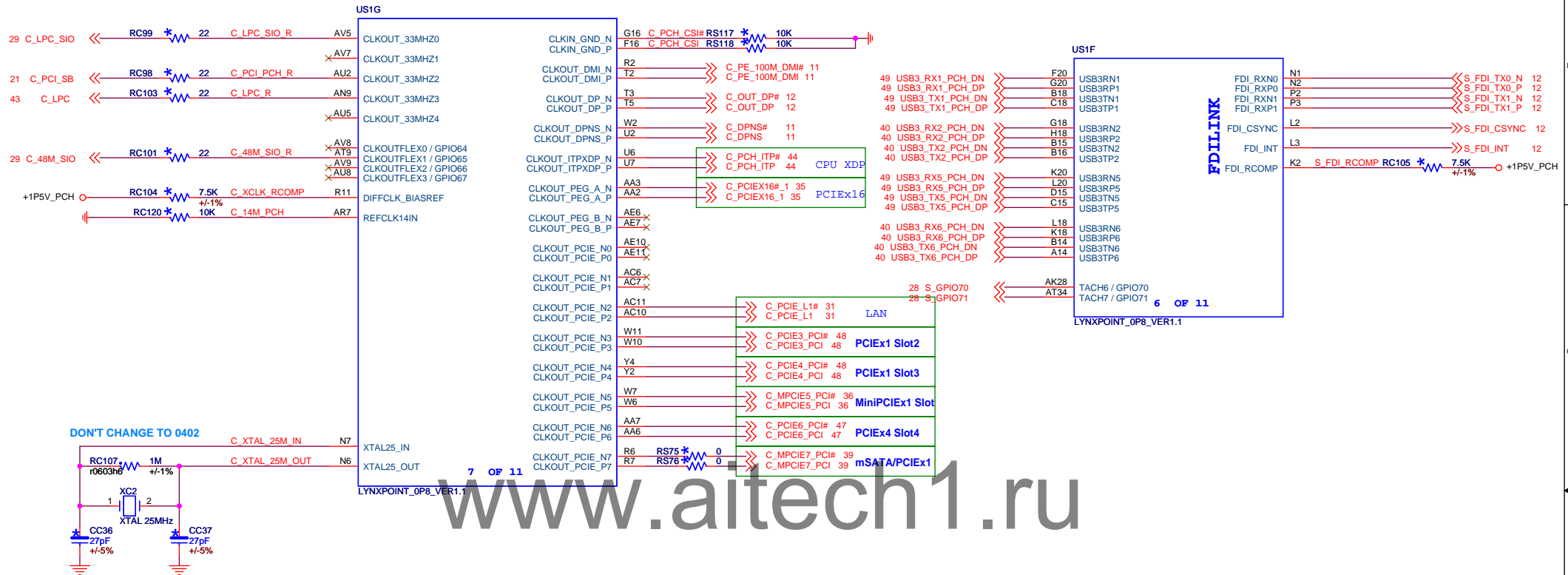
**Rev**  
**A00**

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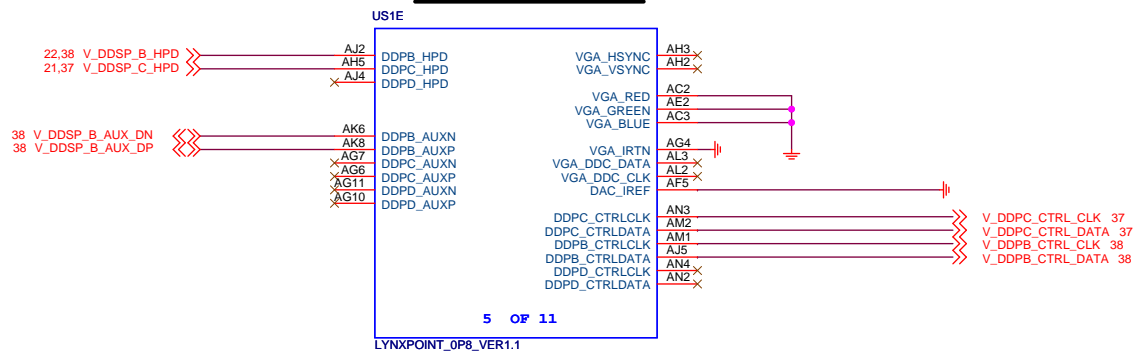




## PCH - CLOCK DISTRIBUTION



## PCH - DP AND RGB

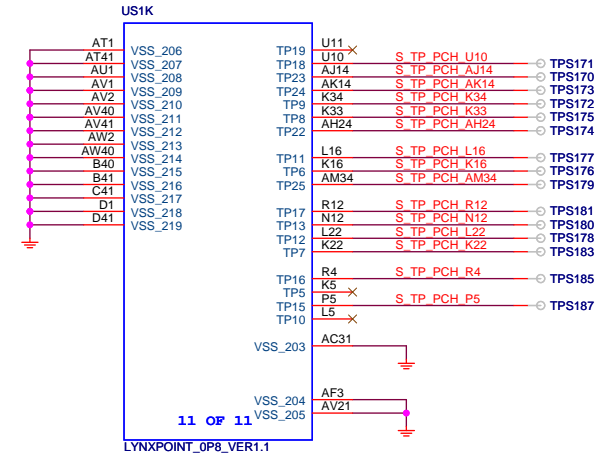
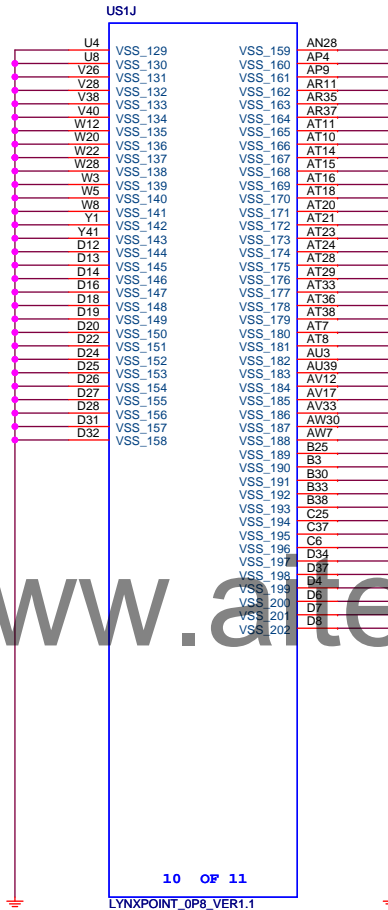
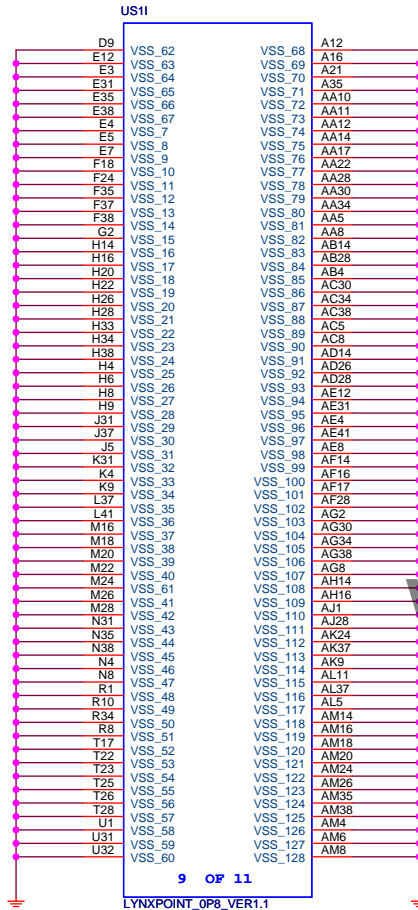


Title  
**PCH-4: VGA/USB3/CLK/FDI**

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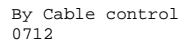
## Chassis Intruder



## ME Disable (Flash override)



## Chassis Intruder

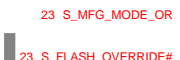


```
22,46 S_GPI_CHASSIS_ID0
22,46 S_GPI_CHASSIS_ID1
22,46 MT/ST_ID
```



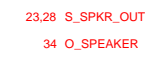
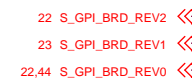
## ME Disable (Flash override)

20100127: Need to check  
this schematic



**BEEP**

Rev2	Rev1	Rev0	Type
0	0	0	Default
0	0	1	Reserved
0	1	0	Reserved
0	1	1	Reserved
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved



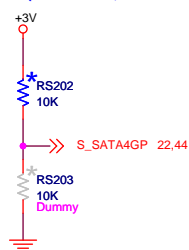
### PCH-8: MISC CONN/BEEP/ID

<b>Goodyear</b>	<b>A00</b>	
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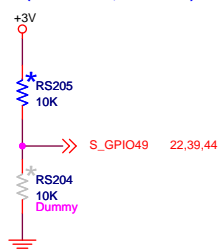
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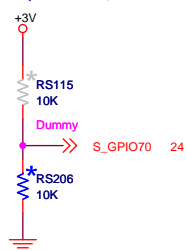
GPIO16 (H-&gt;SATA4 ; L-&gt;PCle1)



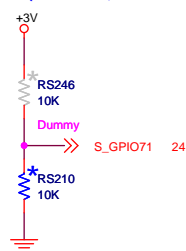
GPIO49 (H-&gt;SATA5 ; L-&gt;PCle2)



GPIO70 (H-&gt;PCle1 ; L-&gt;USB3 3)

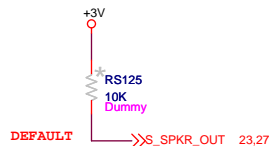


GPIO71 (H-&gt;PCle2 ; L-&gt;USB3 4)



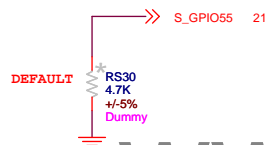
No Reboot Mode

SPKR (IN-PD)	Description
High	No reboot mode: Enable
Low	No reboot mode: Disable



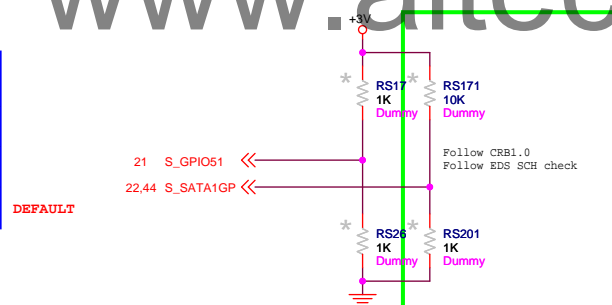
Topblock Swap Mode

GPIO55 (IN-PU)	Description
High	Topblock swap mode: Disable
Low	Topblock swap mode: Enable



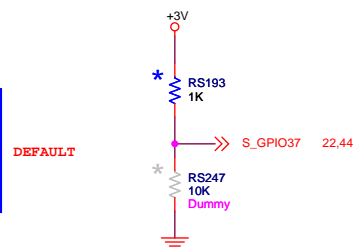
Boot BIOS Destination Selection

GPIO51 (IN-PU)	SATA1GP/GP19 (IN-PU)	Description
Low	Low	Flash cycle routed to LPC
High	Low	Flash cycle routed to PCI
High	High	Flash cycle routed to SPI



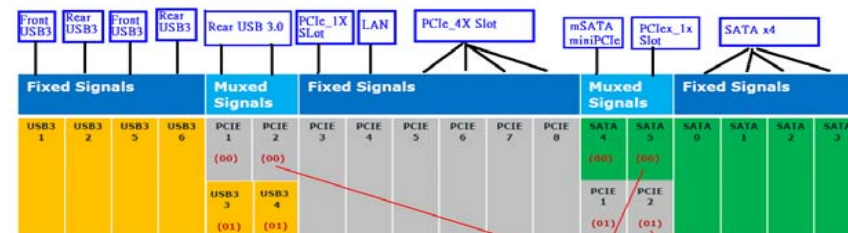
TLS Confidentiality

GPIO37 (IN-PD)	Description
High	ME Crypto TLS cipher suite with confidentiality
Low	ME Crypto TLS cipher suite with no confidentiality



## Lynx Point I/O Flexibility

- New architecture allows some I/O Ports to be configured at time of system design



- I/O Flexibility is configured via soft strap

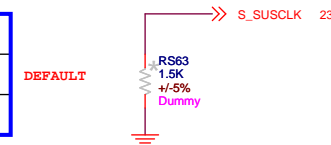
GPIO70	GPIO71
0: USB3 3	0: USB3 4
1: PCIe 1	1: PCIe 2

GPIO16	GPIO49
0: PCIe 1	0: PCIe 2
1: SATA 4	1: SATA 5

00b or 01b: Assign muxed signal to desired port  
10b: Reserved  
11b: Assign desired port based on GPIO  
Example of soft strap settings

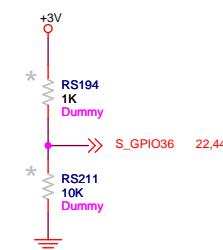
On-Die PLL Voltage Regulator

GPIO62/SUSCLK (IN-PU)	Description
High	Regulator is enabled.
Low	Regulator is disabled.

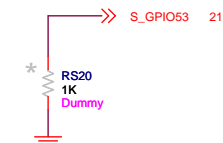


DMI Rx Termination

GPIO36 (IN-PD)	Description
Low	DMI Rx Termination Voltage



DMI AC COUPLING FULL VOLTAGE MODE  
WHEN SAMPLED LOW



Title

PCH-9: STRAP OPTION

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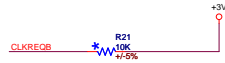




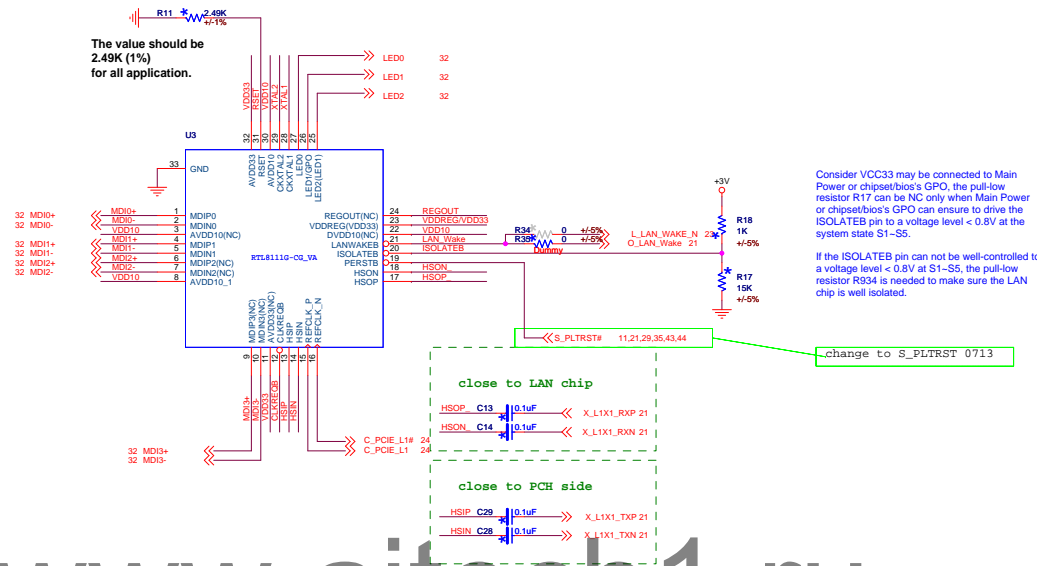
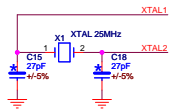
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Title		
SIO-SCH5555-2		
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R21, R22 could be saved through sharing the pull-up resistors which might be possibly existed on the motherboard already.

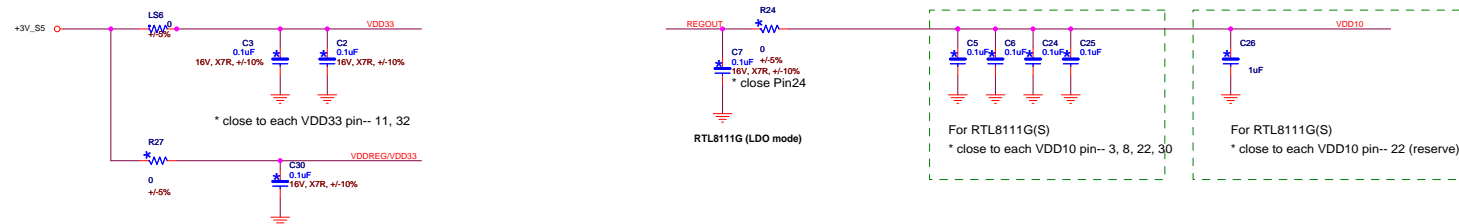


Note: 10K ohm close to Host side

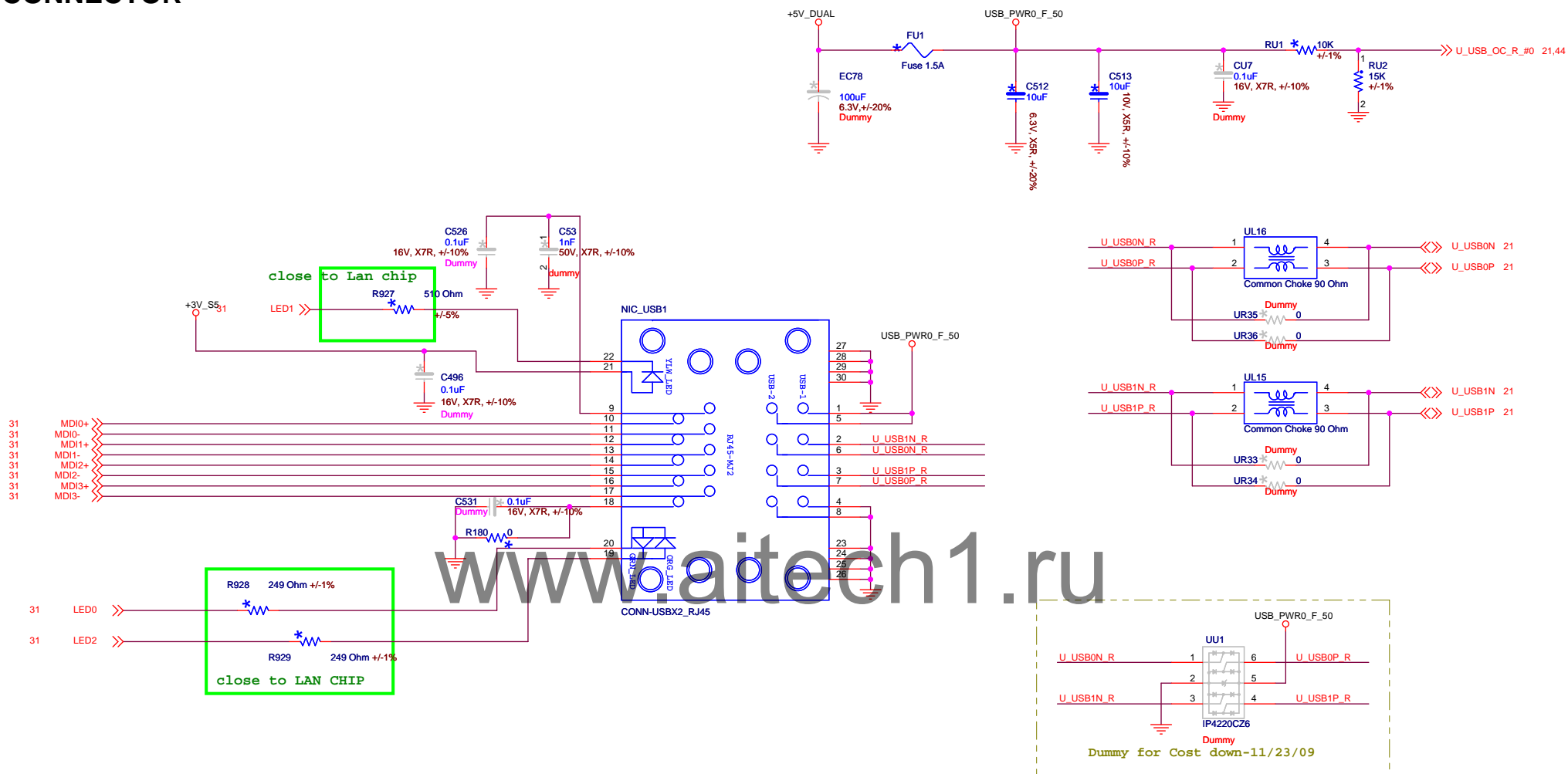


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## LAN POWER



# LAN CONNECTOR

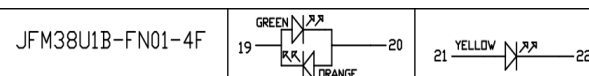


SPEED LED	
LINK 10M	GREEN
LINK 100M	
LINK 1000M	ORANGE

ACTIVE LED

YELLOW = LINK UP  
BLINKING = TX/RX ACTIVITY

JFM38U1B-FN01-4F



When implementing customized LEDs:

Configure IO register offset 18h~19h to support your own LED signals. For example, if the value in the IO offset 0x18 is 0x0CA9h (0000110010101001b), the LED actions are:

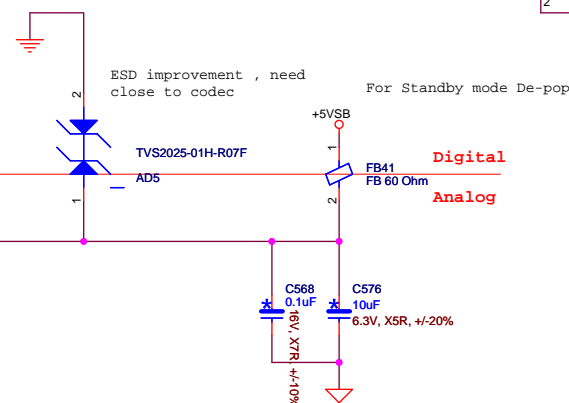
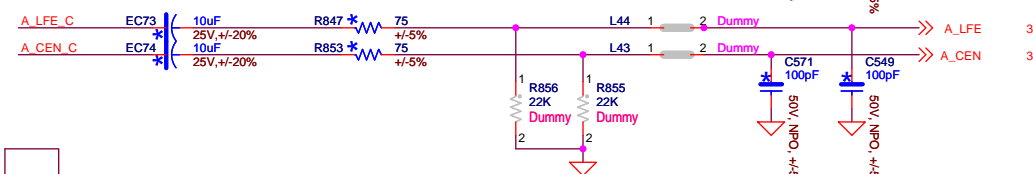
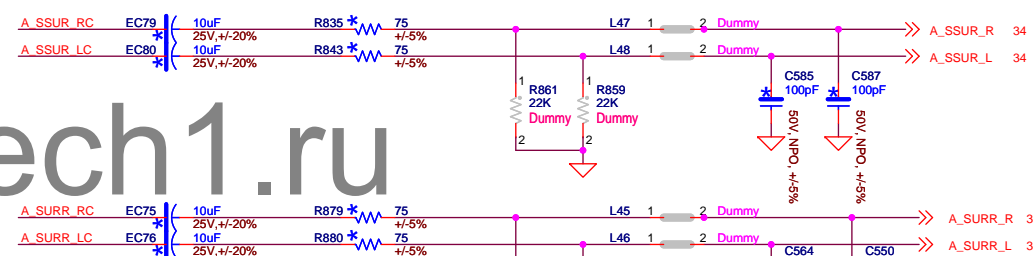
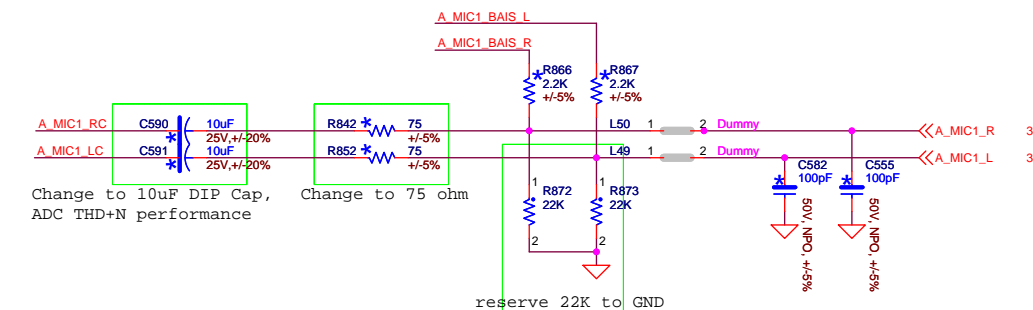
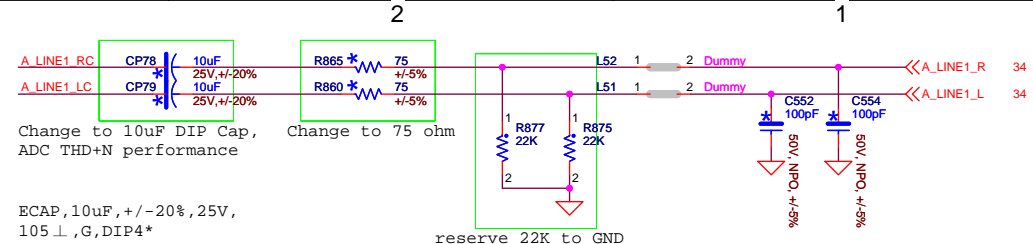
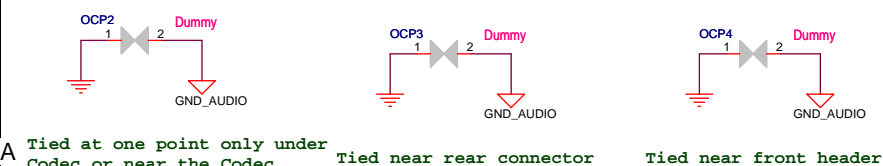
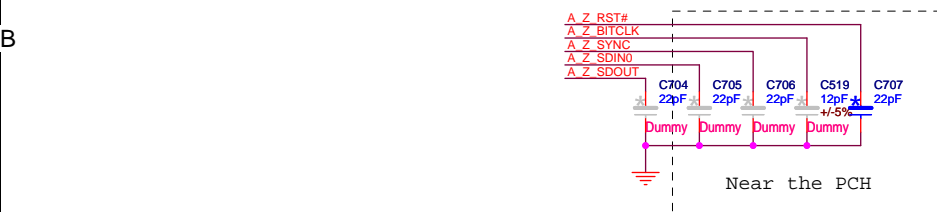
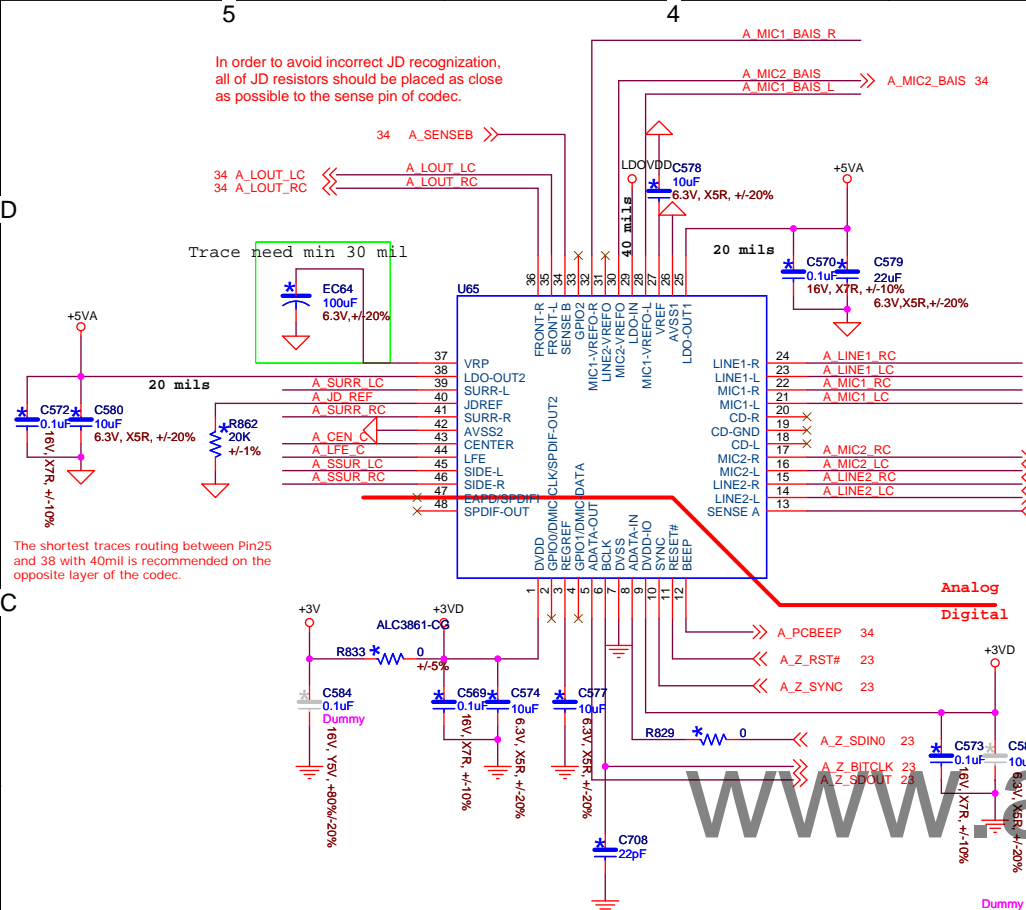
- LED 0: On only in 10M mode, with blinking during TX/RX
- LED 1: On only in 100M mode, with blinking during TX/RX
- LED 2: On only in 1000M mode, with blinking during TX/RX



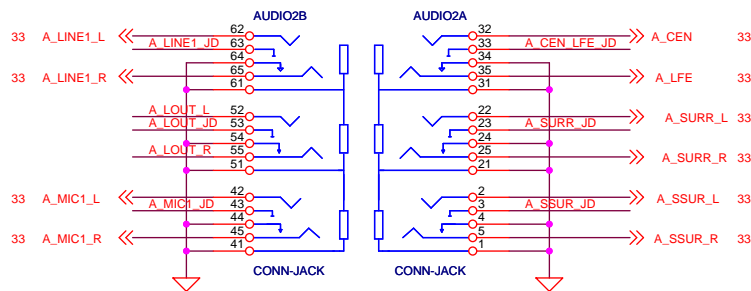
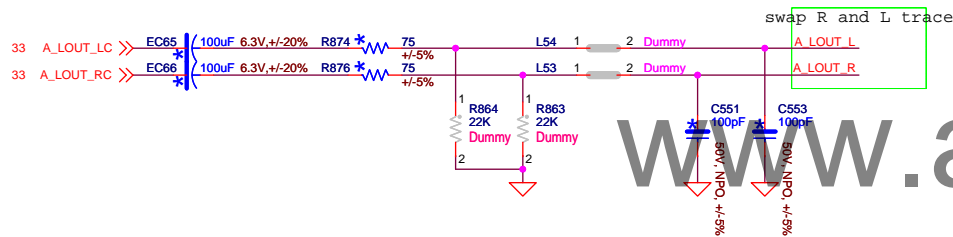
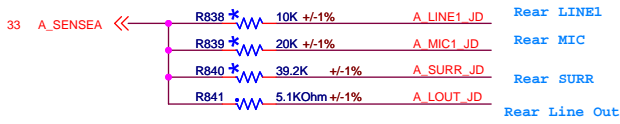
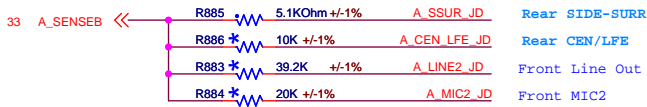
Title  
**LAN Power & LAN/USB Conn**

DWG NO  
**Goodyear**

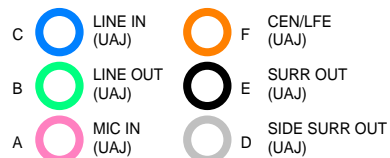
Date: 星期三, 二月 20, 2013 Sheet 32 of 57



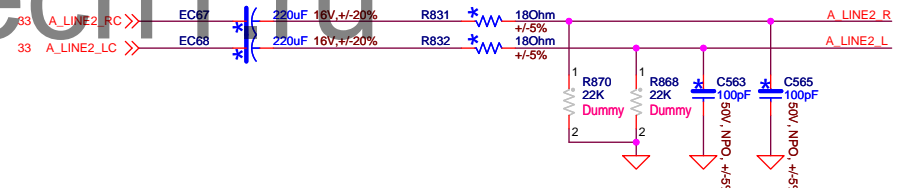
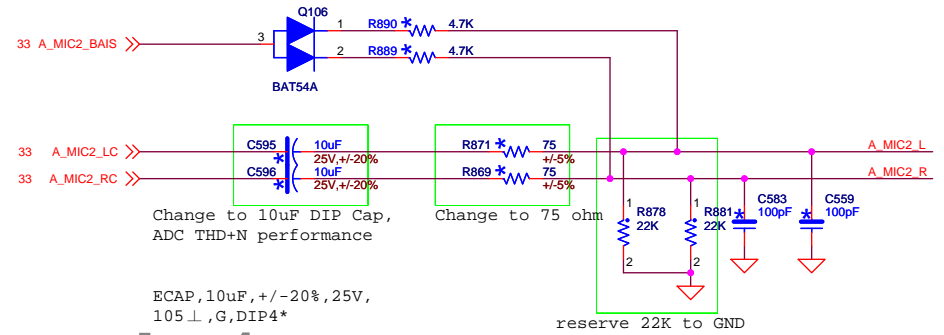
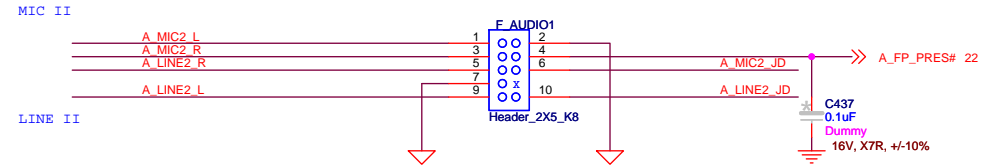
# JACK SENSE



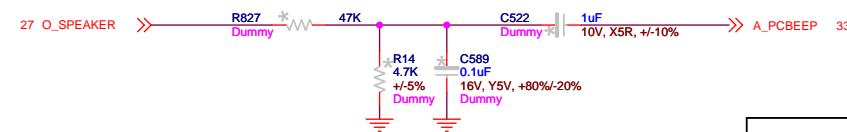
Audio Jack



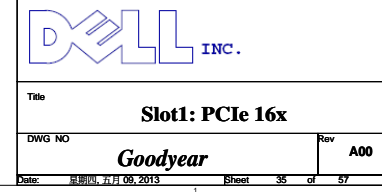
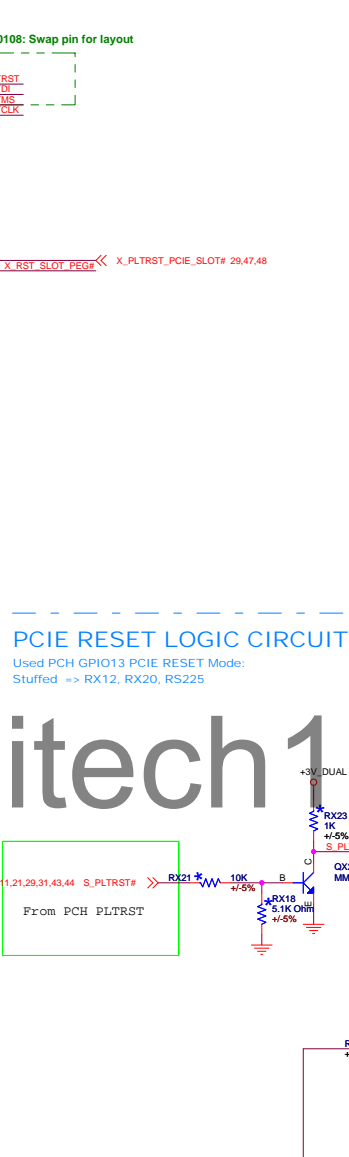
# Front\_Audio



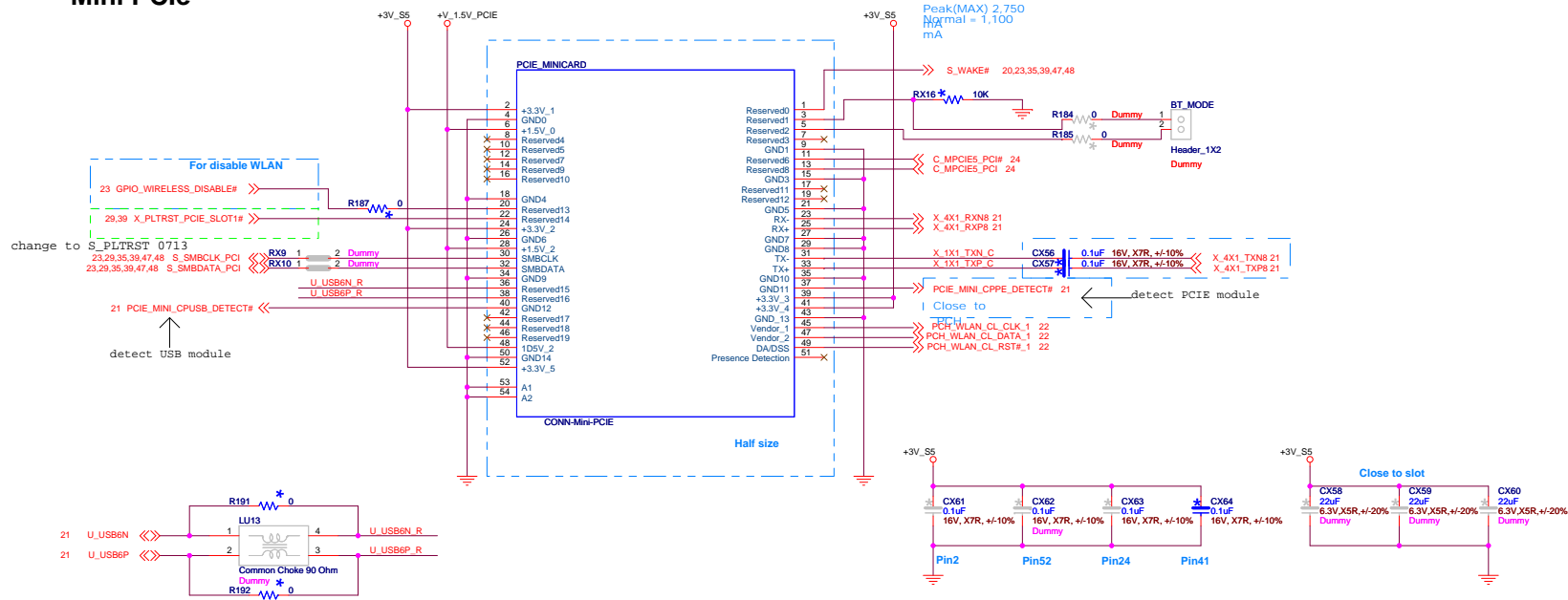
# PC BEEP



Title	
Audio Conn	
DWG NO	Rev
Goodyear	A00
Date: 星期三, 三月 20, 2013	Sheet 34 of 57

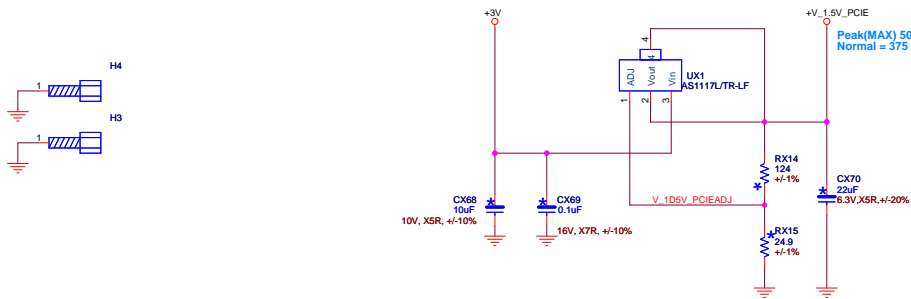


# Mini PCIe



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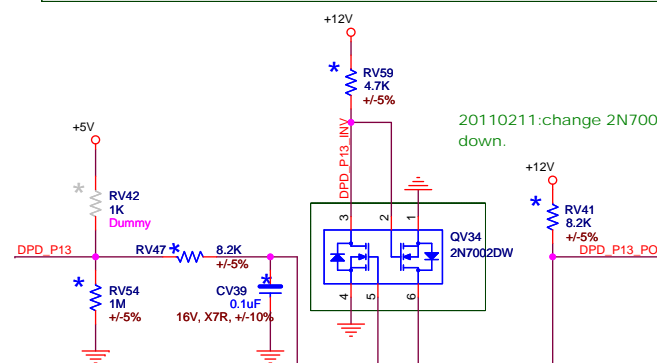
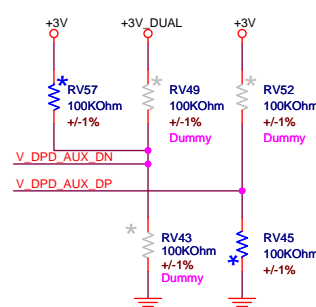
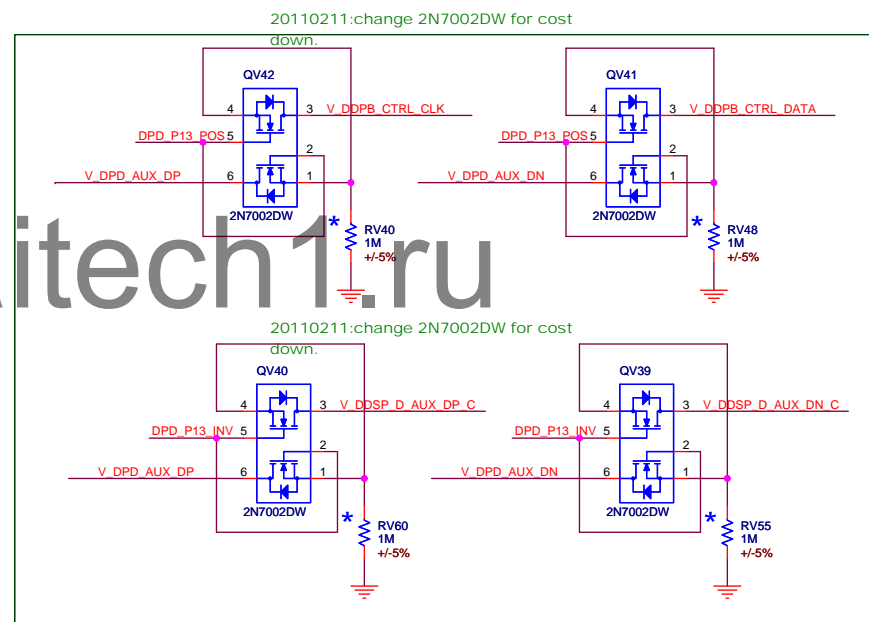
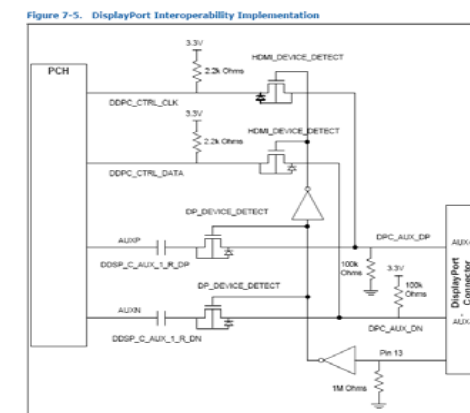
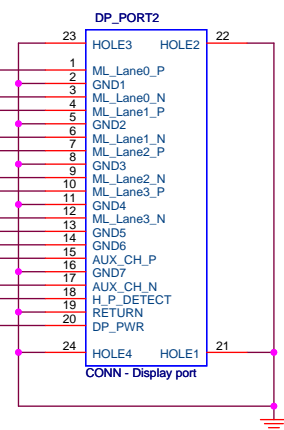
## Latch



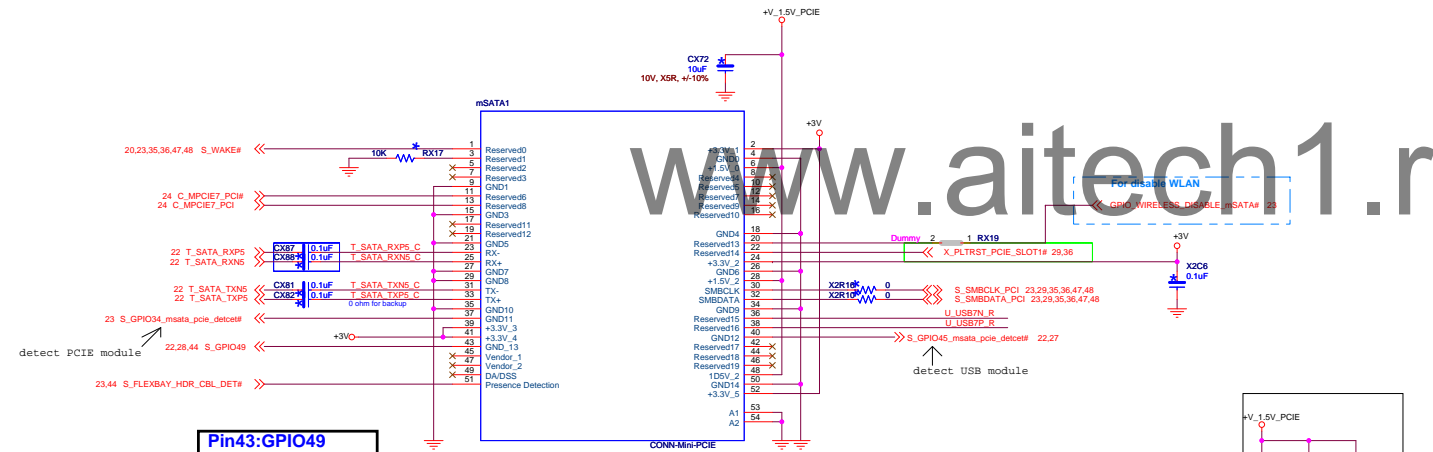
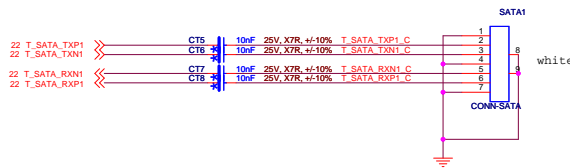
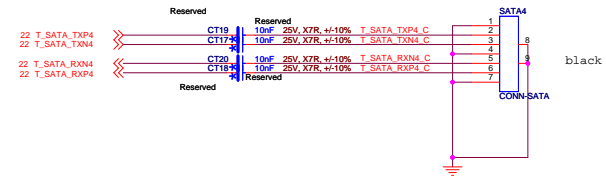
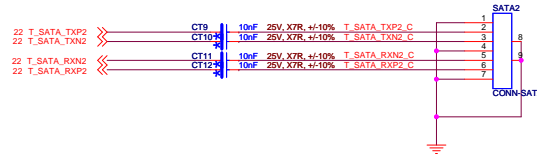
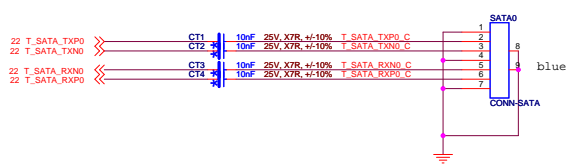
<b>DELL INC.</b>	
Title <b>Mini PCIe</b>	
DWG NO <b>Goodyear</b>	Rev <b>A00</b>
Date: 星期三, 三月 20, 2013	Sheet 36 of 57







# SATA x 4



Pin43:GPIO49  
mSATA -->NC  
mini PCIe -->GND

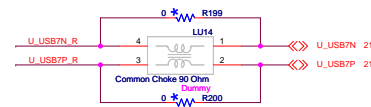
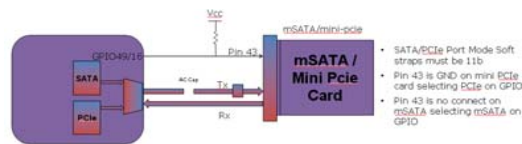
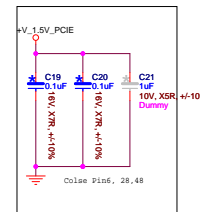
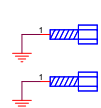
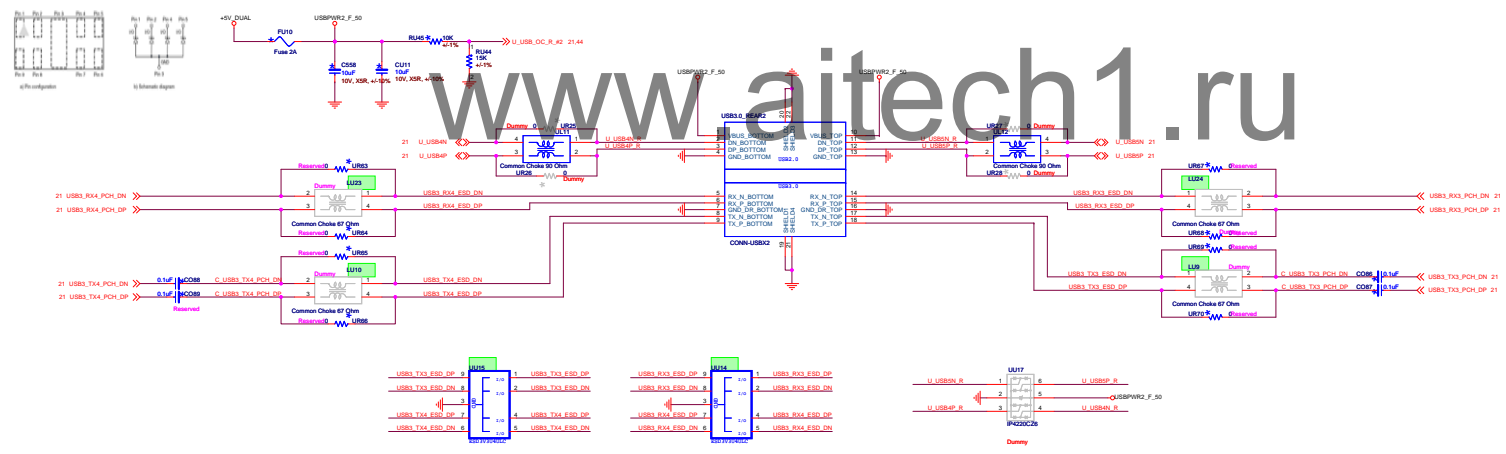
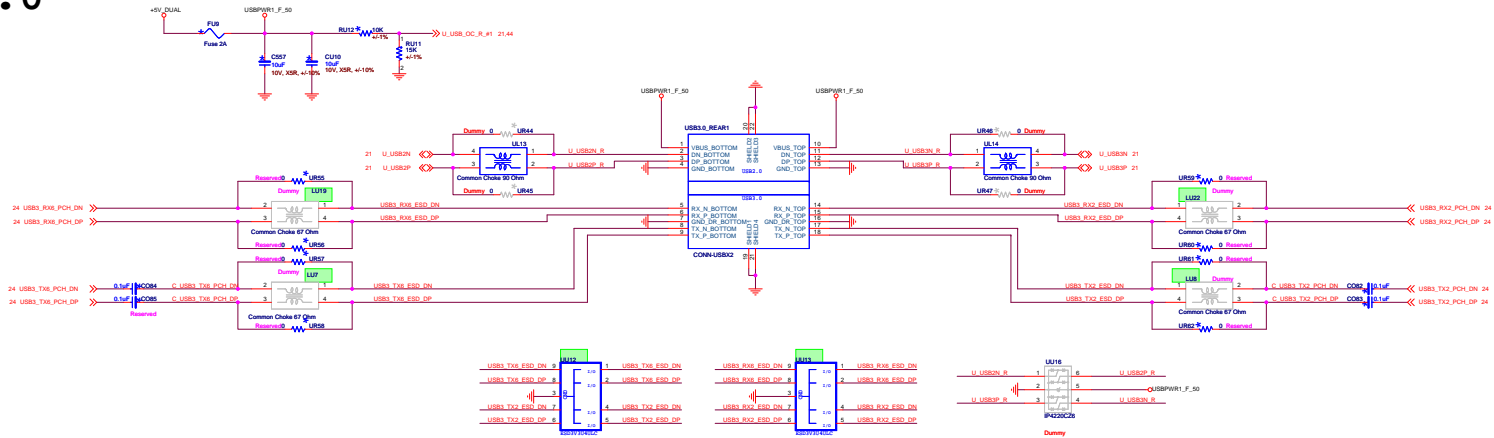


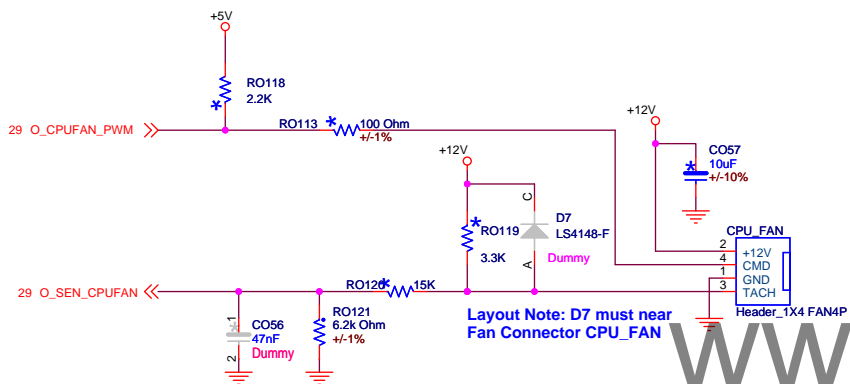
Table below summarizes the AC cap requirement on the motherboard when using SATA/PCIe mixed port.

Condition	PCIe only	SATA only	PCIe/SATA
PCH Tx	100 nF	10 nF	100 nF
PCH Rx	None	10 nF (Can be removed if choose NOT to support DC coupled ODDs)	None (not footprint and stuff with zero ohm for backup)

Rear USB3.0

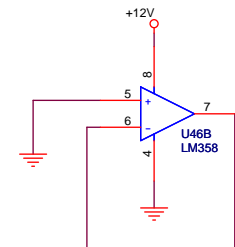
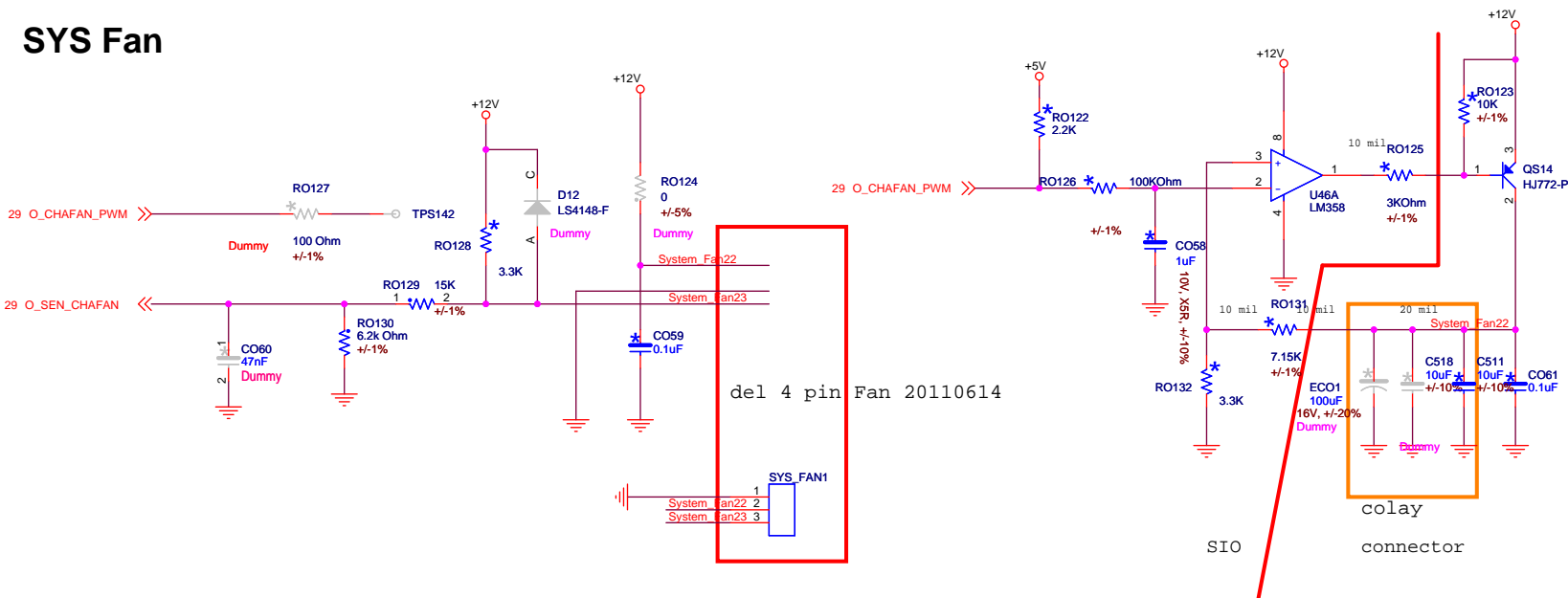


## CPU Fan



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**SYS Fan**



del 4 pin Fan 20110614

SIO

colay  
connector

Title

**FAN**

DWG NO
--------

**Goodyear**

Rev	<b>A00</b>
-----	------------

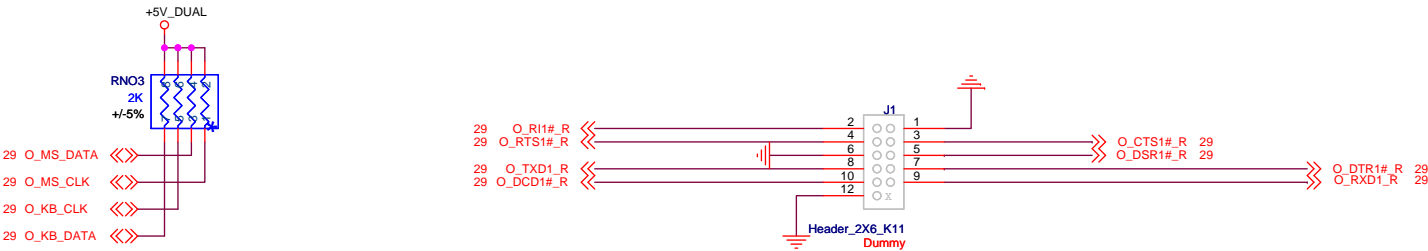
Date: 星期三, 二月 20, 2013

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Serial

PS2 port

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Title			Serial / PS2 port	
DWG NO		Goodyear		Rev A00
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## SPI

Follow PDG 1.0  
0712

## LPC DEBUG

### LPC\_DEBUG

Dummy

## SPI\_8MB

變更文字為SPI\_2，為改打SMD  
20120216: SPI1 Change to WINBOND\_W25Q32BVSSIG

SPI\_2

<LB>  
Label for 686BIOS AMI  
<Tolerance>  
BIOS\_Label

W25Q64FVSSIG

<LB>  
Label  
<Tolerance>  
2D\_Label

CLOSE TO SPI  
If socket not use ,need change to SMD Type

Follow PDG 1.0  
0712

+3V

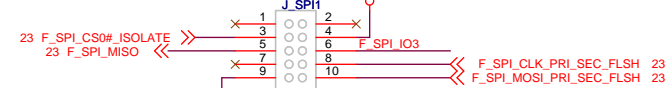
R20  
1K

+/-5%

R22  
1K

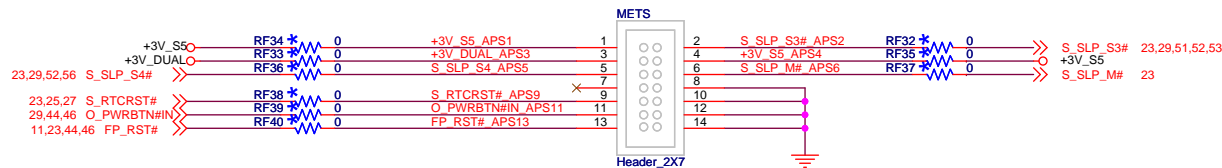
+/-5%

F\_SPI\_IO3  
F\_SPI\_IO2



for SPI connector using

## APS DEBUG



Desktop		
APS Connector	Pin	Meaning
Pin 1	VccSus3_3	3.3 V Suspend Power Well
Pin 2	SLP_S3#	When asserted (0) system is in S3
Pin 3	VccDSW3_3	Used to determine if system is in Deep Sx
Pin 4	VccSus3_3	When off (0) system is in S5
Pin 5	SLP_S4#	When asserted (0) system is in S4
Pin 6	SLP_A#	When asserted (0) ME is in Moff
Pin 7		Unused
Pin 8	GND	Ground
Pin 9	RTCST#	When asserted (0) CMOS is cleared
Pin 10	GND	Ground for RTCST#
Pin 11	PWRBTN#	When asserted (0) Power Button Pushed
Pin 12	GND	Ground for PWRBTN#
Pin 13	SYS_RESET#	When asserted (0) Reset Button Pushed
Pin 14	GND	Ground for SYS_RESET#

DELL INC.

Title

SPI/LPC DBG

DWG NO

Goodyear

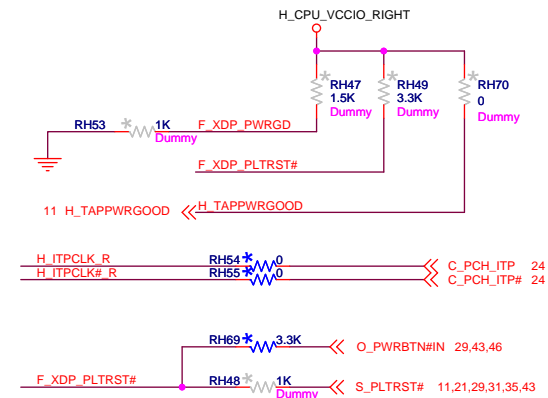
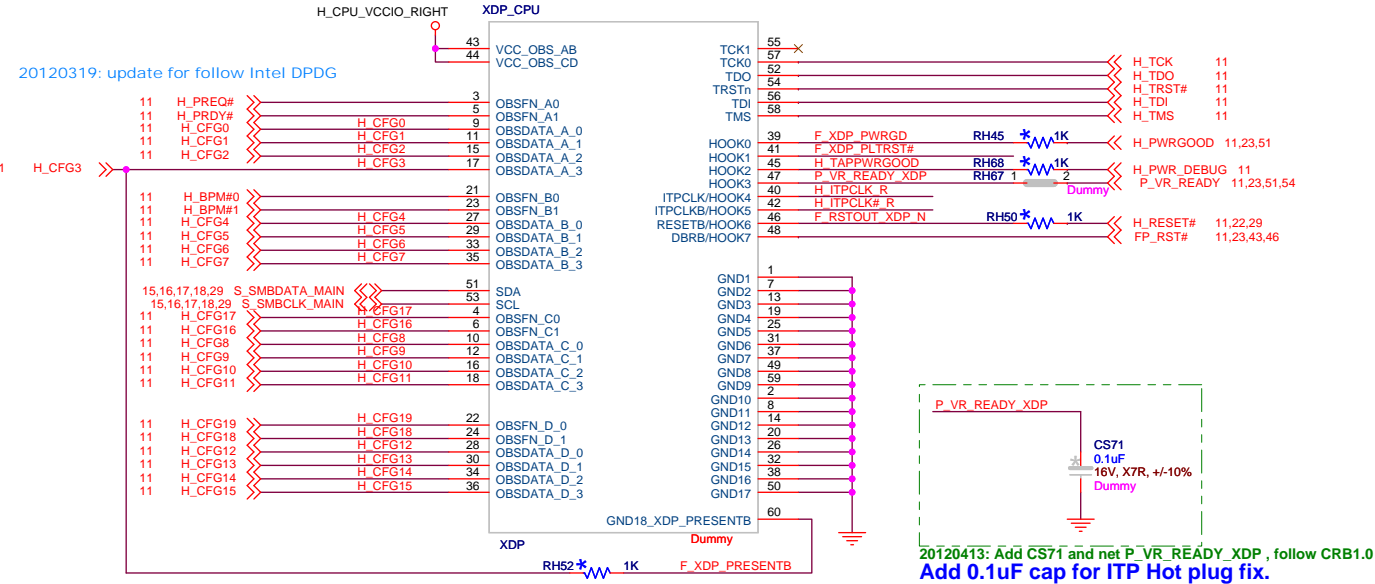
Rev

A00

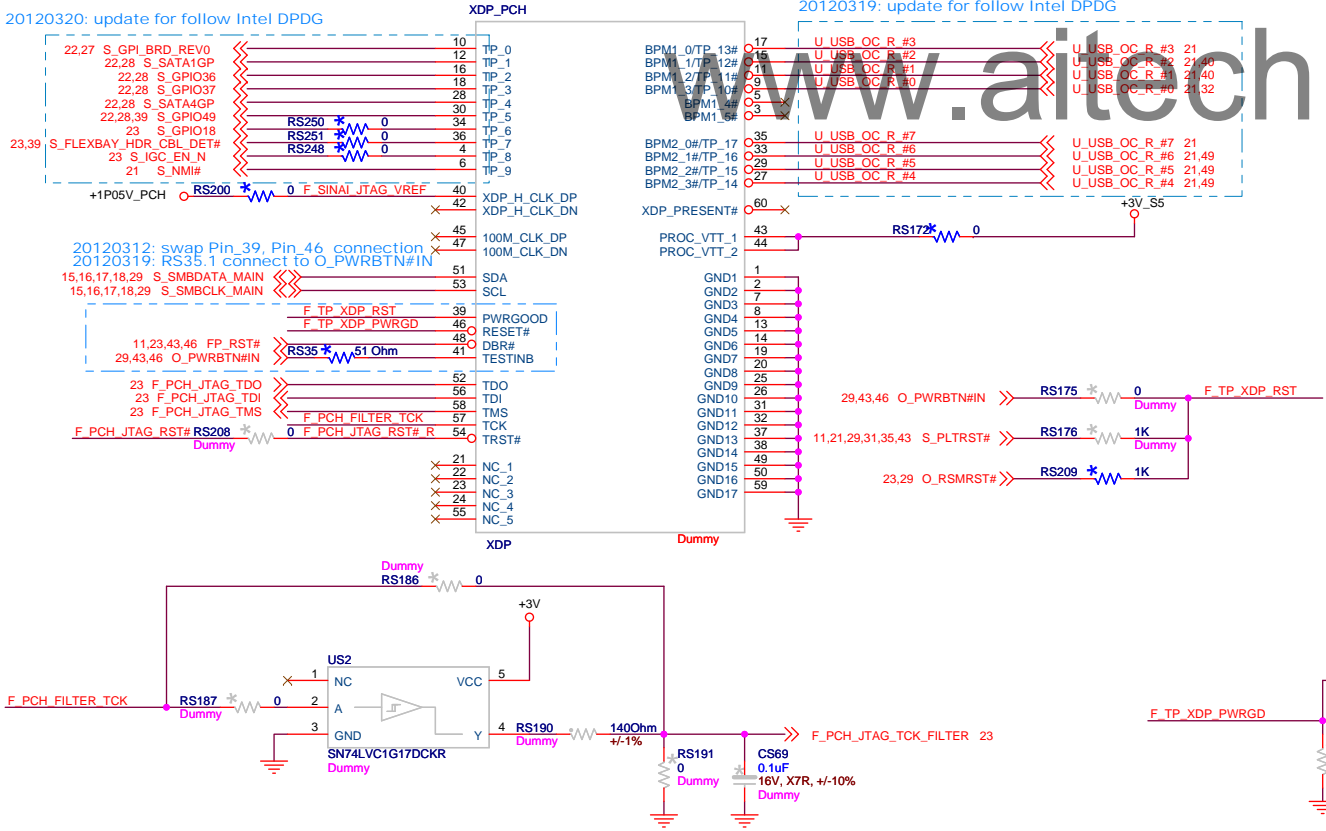
Date: 星期三, 二月 20, 2013

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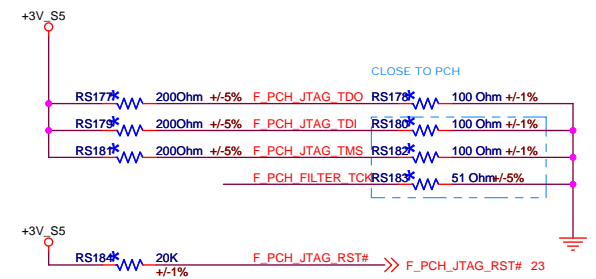
XDP Connector - CPU




XDP Connector - PCH



2009/12/21 Update JTAG Table	PCH JTAG Enable		PCH JTAG Disable	
	ES1	ES2	ES1	ES2
F_PCH_JTAG_TDO	RS177	No Stff	200 Ohms <sup>1</sup>	No Stuff
	RS178	No Stff	100 Ohms <sup>1</sup>	No Stuff
F_PCH_JTAG_TMS	RS179	200 Ohms	200 Ohms	No Stuff
	RS180	100 Ohms	100 Ohms	No Stuff
F_PCH_JTAG_TDI	RS181	200 Ohms	200 Ohms	20K Ohms
	RS182	100 Ohms	100 Ohms	10K Ohms
F_PCH_FILTER_TCK	RS183	51 Ohms	51 Ohms	51 Ohms
F_PCH_JTAG_RST#	RS184	20K Ohms	20K Ohms	No Stuff
	RS185	10K Ohms	10K Ohms	No Stuff





INC.

Title

**XDP**

DWG NO

**Goodyear**

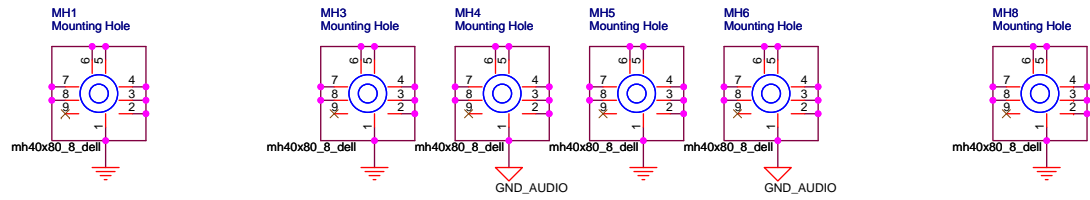
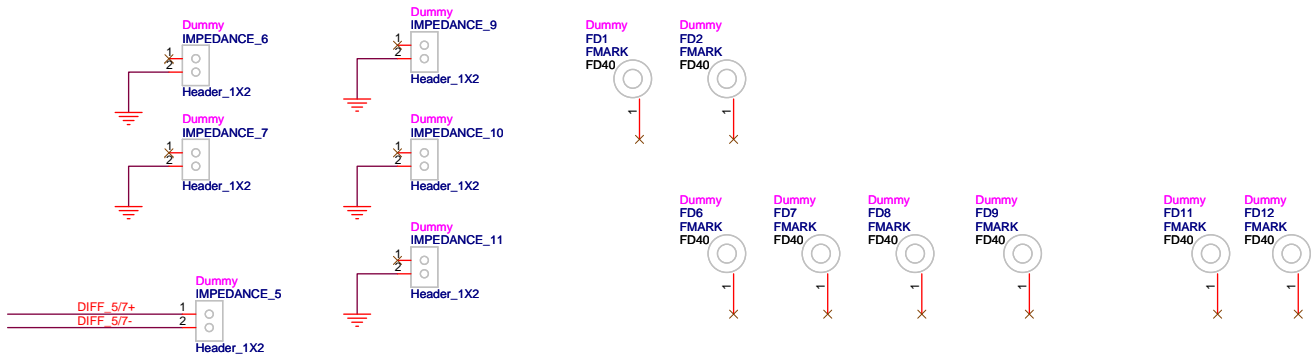
Date: 星期三, 二月 20, 2013

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Rev

**A00**

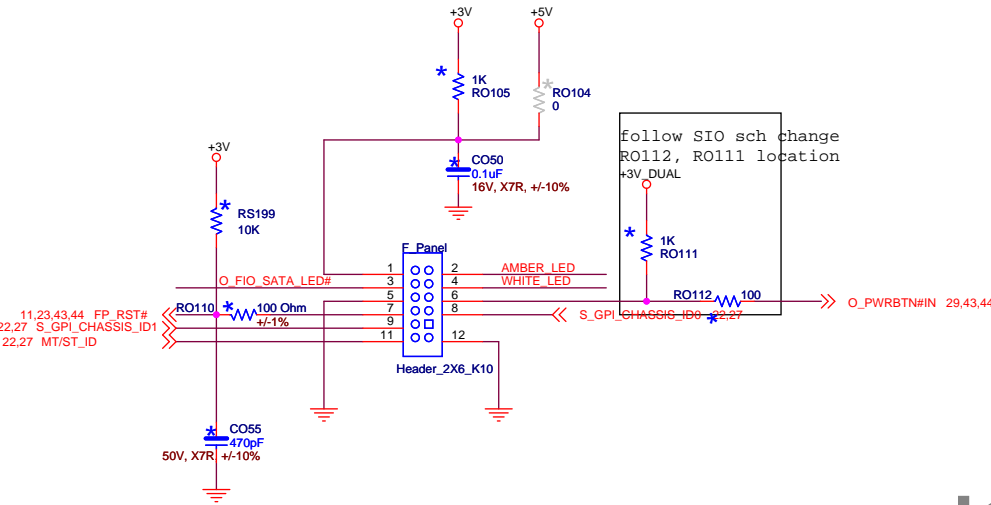




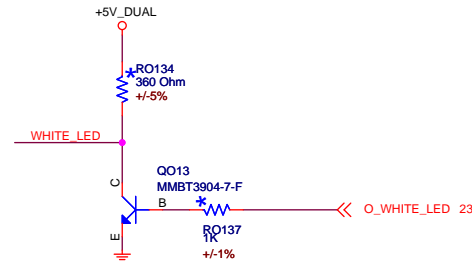
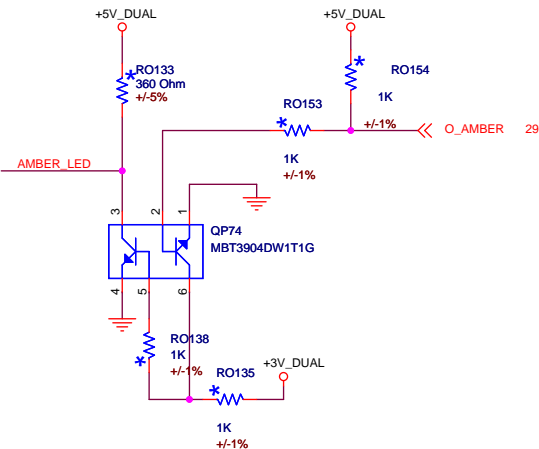
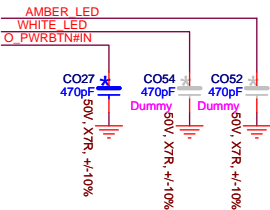
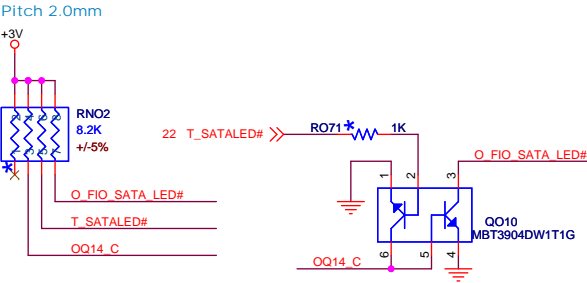
20100108: Add for EMI

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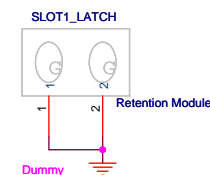
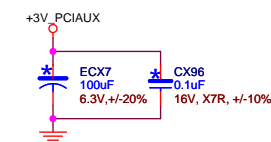
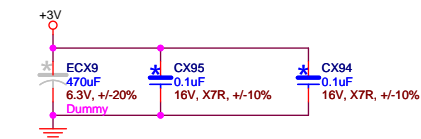
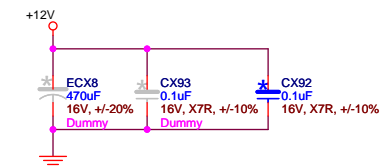
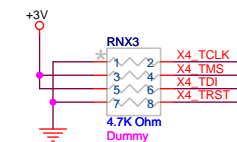
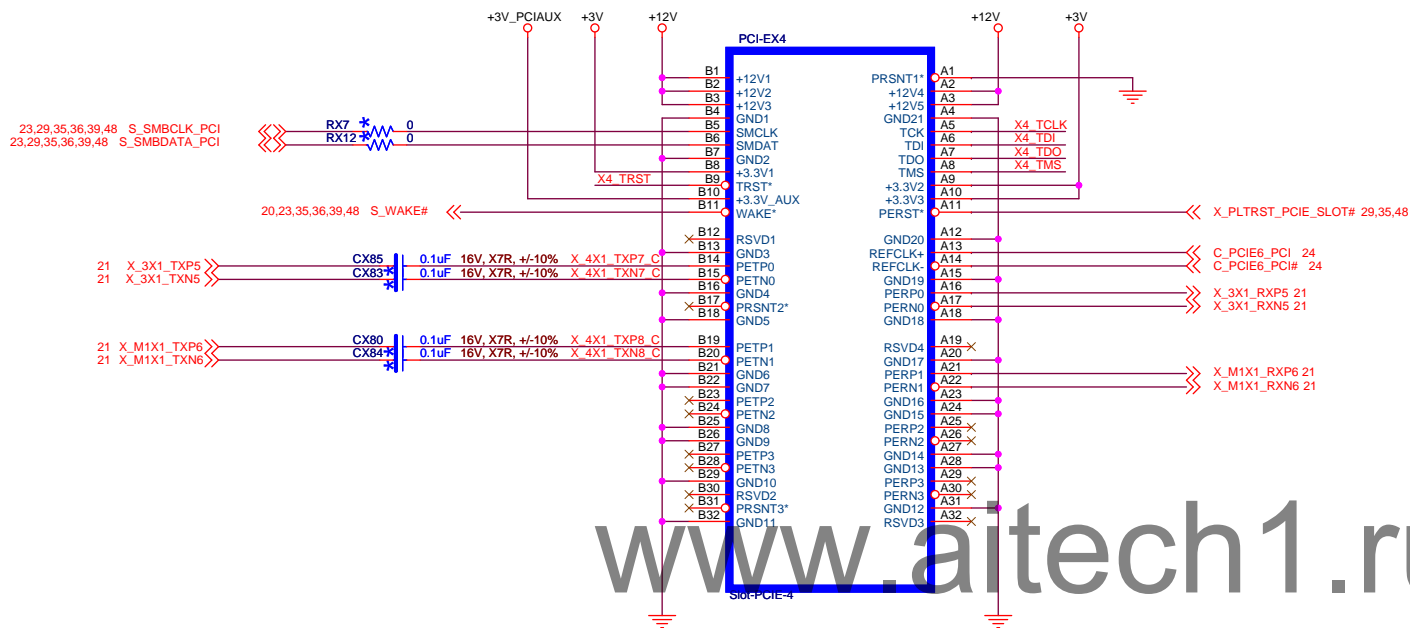
Front\_IO Header




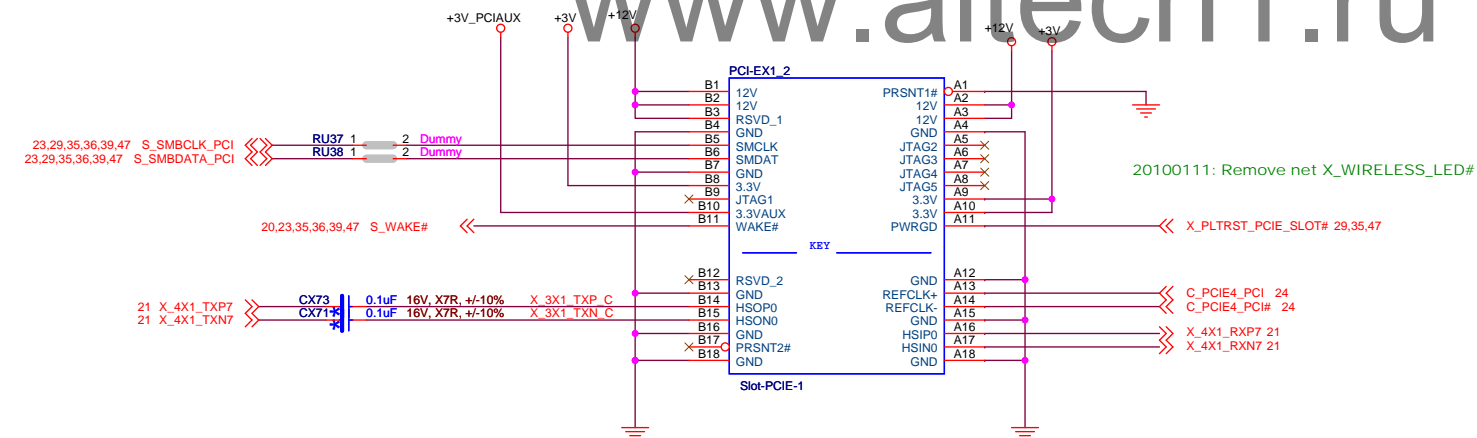
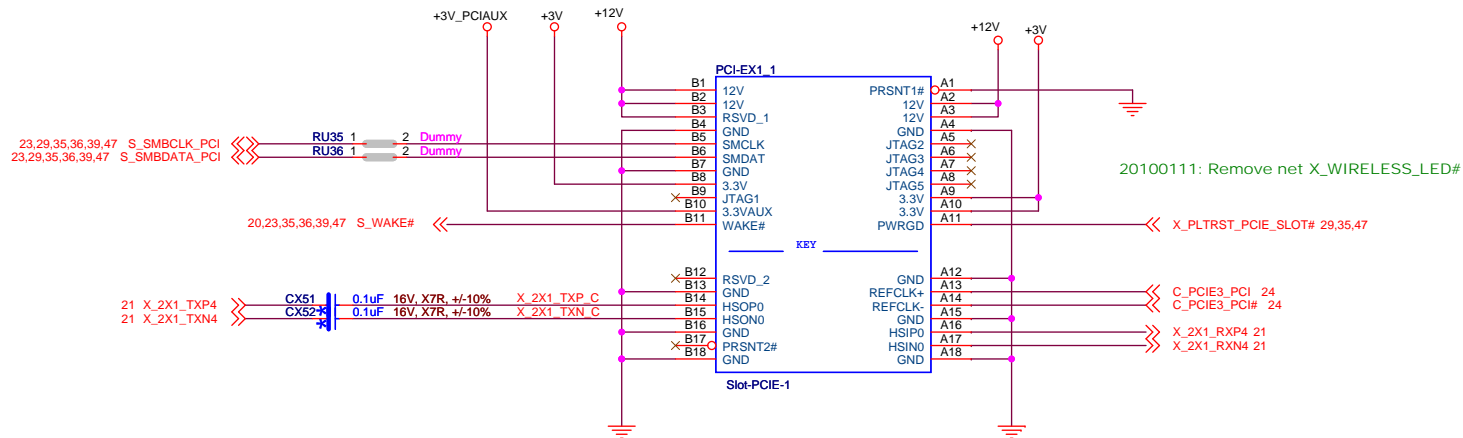
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Title		
Front_Panel		
DWG NO	Goodyear	Rev A00
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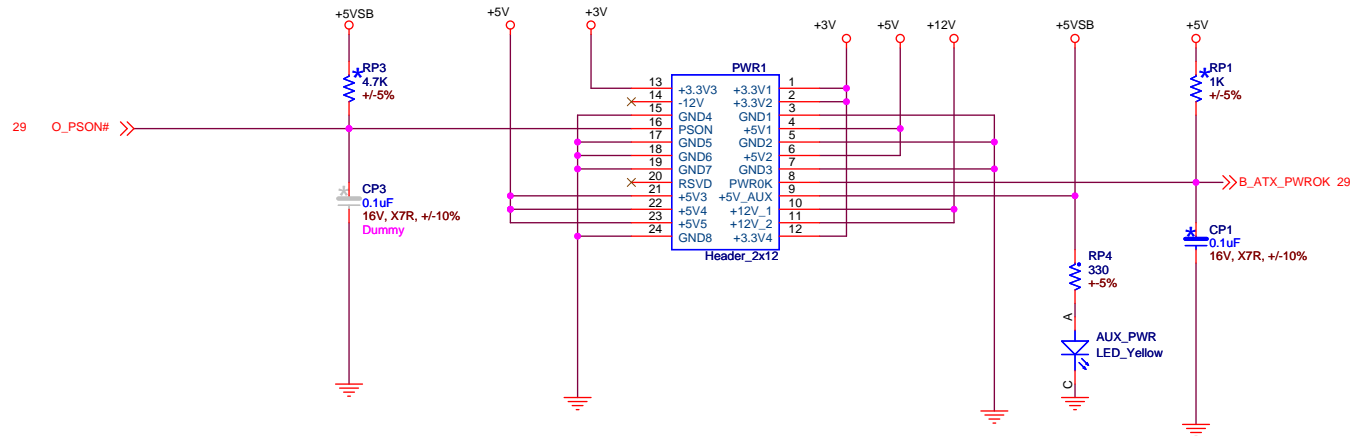


	
Title	
Slot4: PCIe1	
DWG NO	Rev
Goodyear	A00
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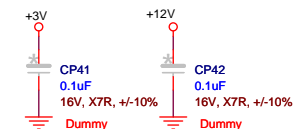
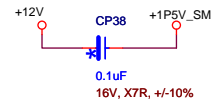
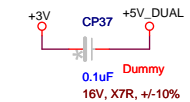
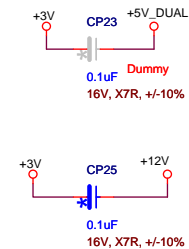
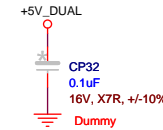
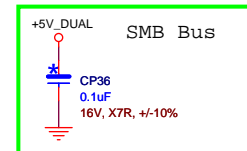
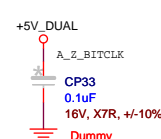
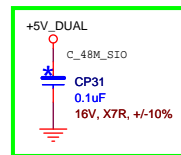
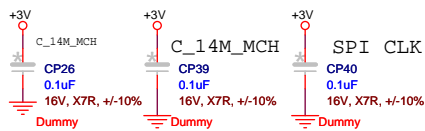
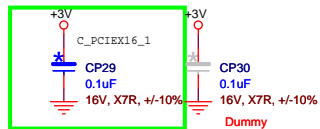
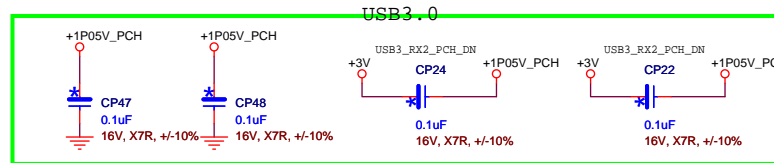
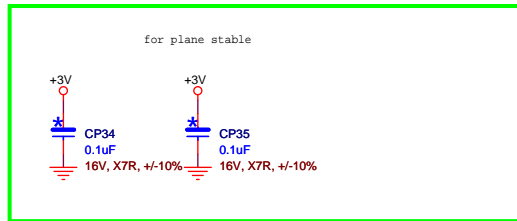




# ATX POWER CONNECTOR



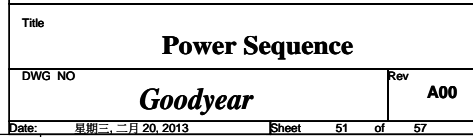
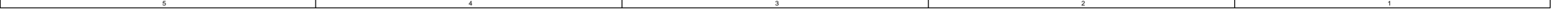
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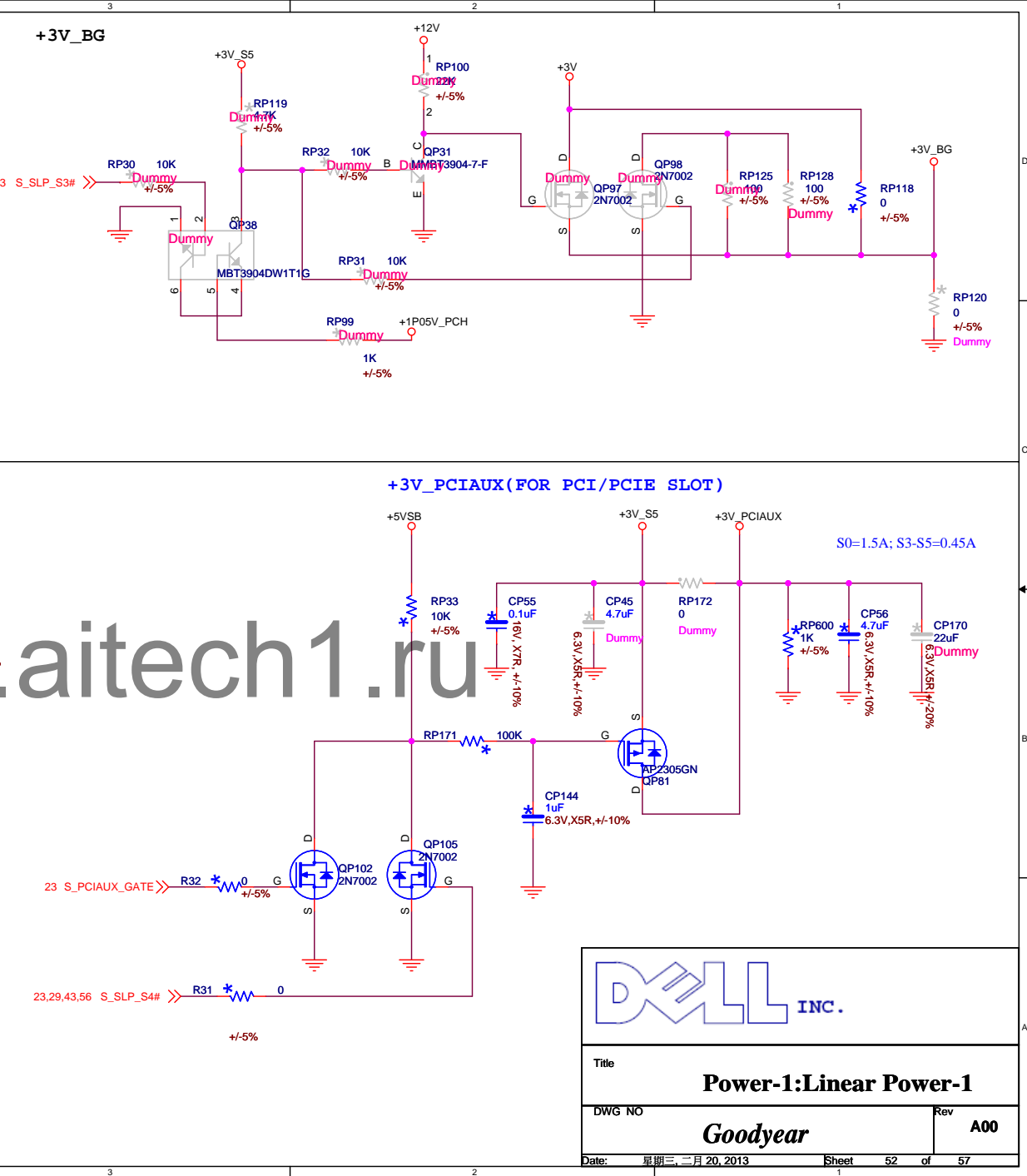
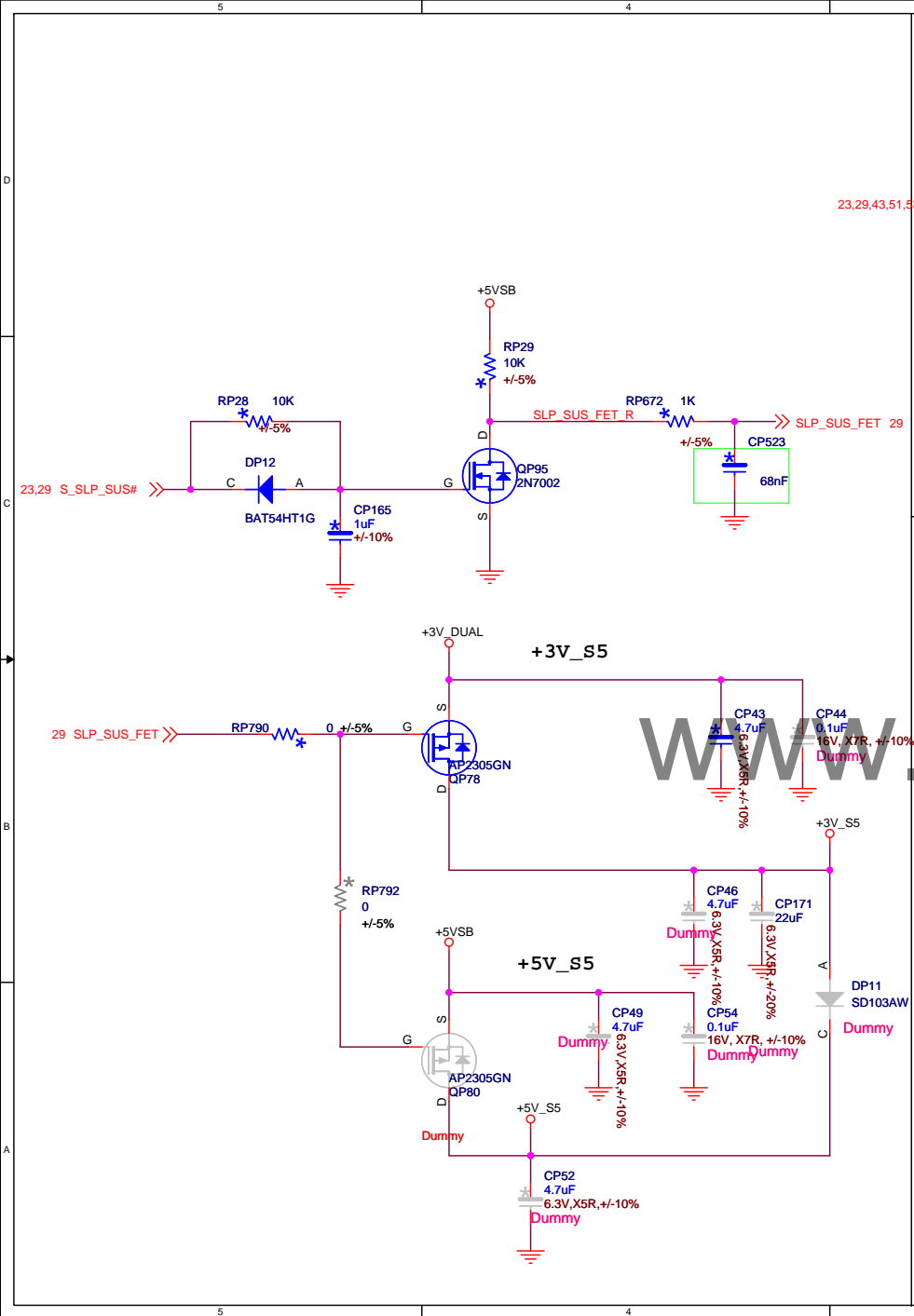


Title		
Power Conn		
DWG NO	Goodyear	Rev A00
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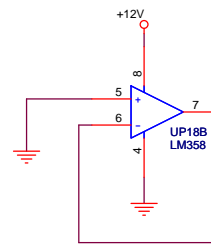
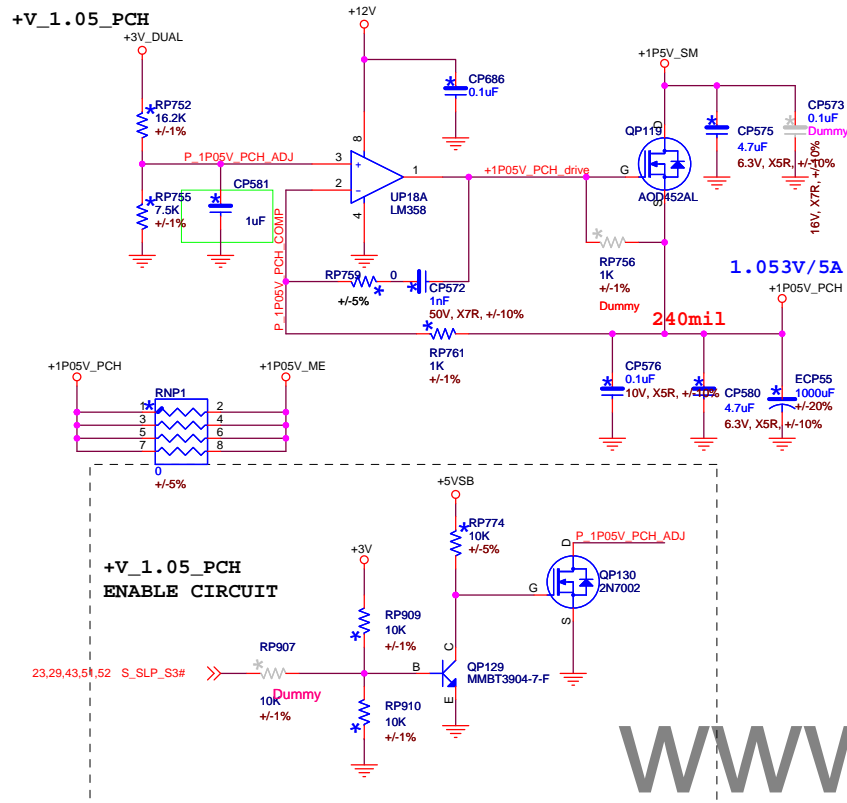
For Deep Sleep

This figure shows a large, empty rectangular area with a light blue background, framed by a black border. The text "For Deep Sleep" is visible in the top left corner. The area is divided into a grid of 5 columns and 1 row, with the columns labeled 1, 2, 3, 4, and 5 from right to left. The rows are labeled C and D from bottom to top.

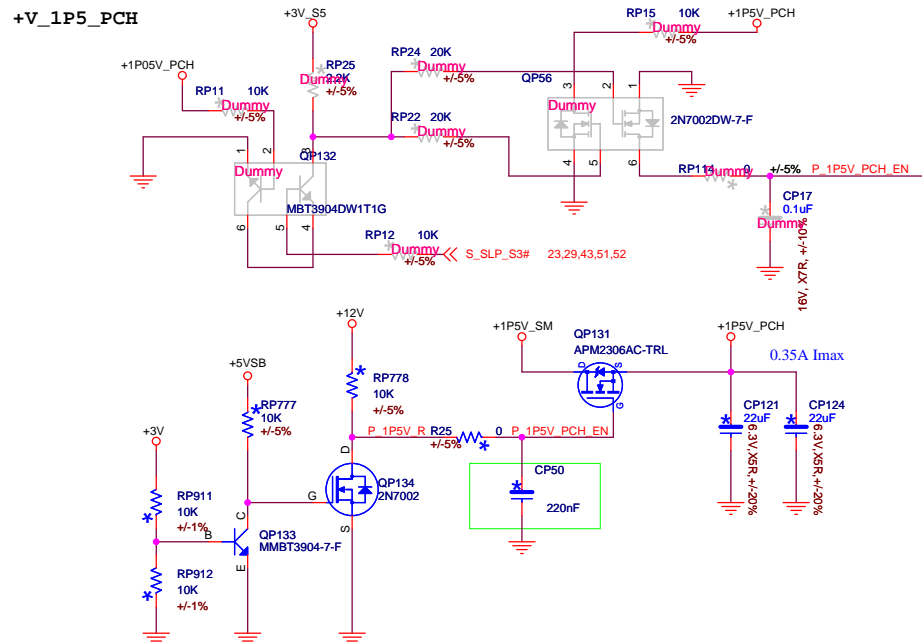








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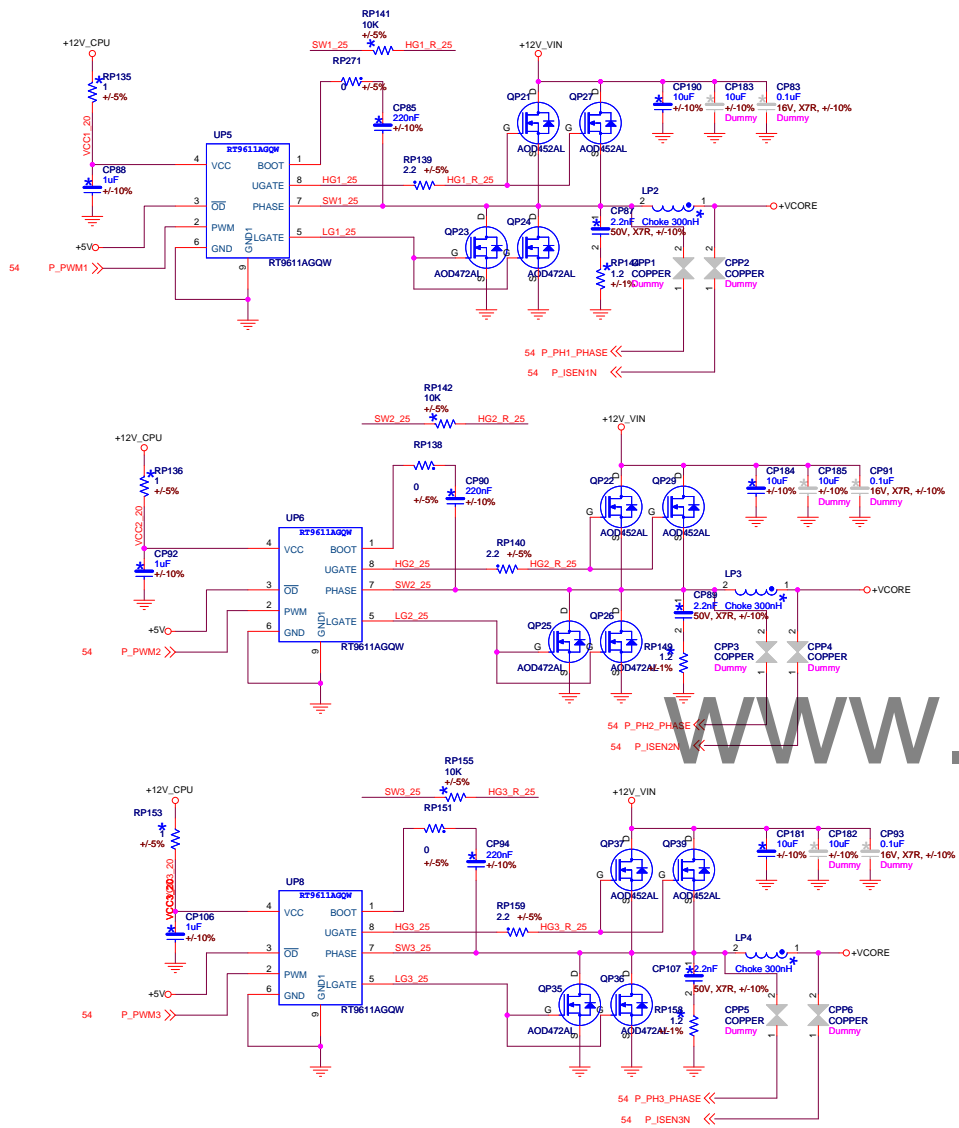


DC Update on 7/16 2012

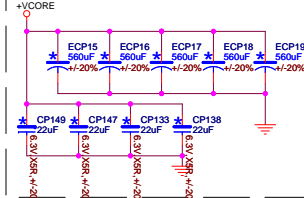
RT8884BGQW

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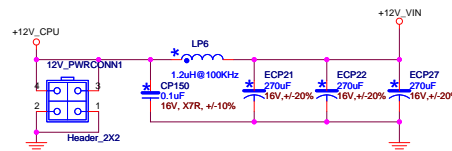
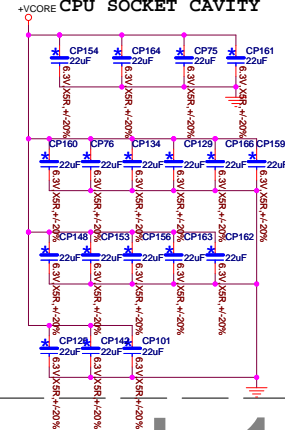
Add sequence control  
follow CRB



**CAD NOTE:**  
**PLACE CAPS AT TOP SOCKET EDGE**

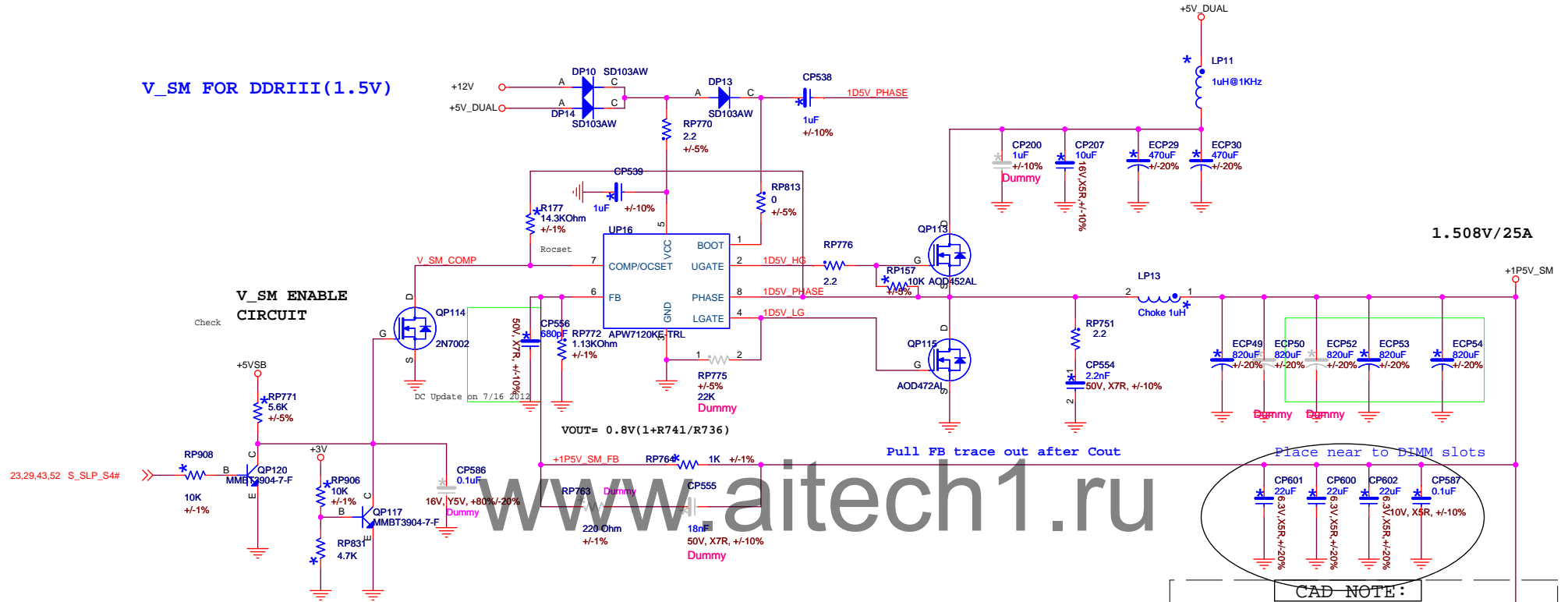


**CAD NOTE:**  
**PLACE ALL 0805 CAPS INSIDE CPU SOCKET CAVITY**

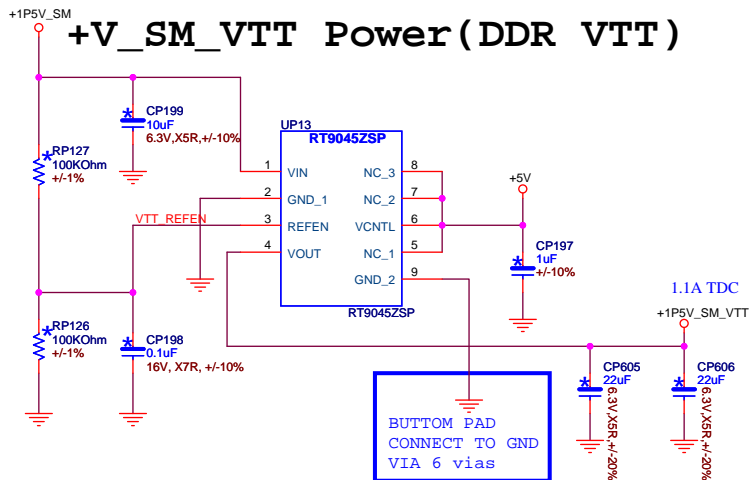


## +V\_1.5\_SM Power(DDRIII)

## V\_SM FOR DDRIII(1.5V)

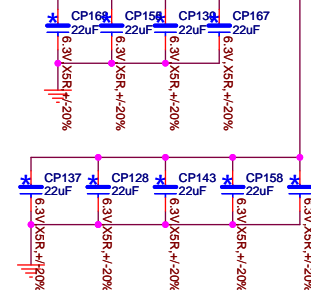


**+V\_SM\_VTT Power (DDR VTT)**



~~CAD NOTE:~~

PLACE ALL 0805 CAPS INSIDE  
CPU SOCKET CAVITY



Title

### Power-6: DDR3

DWG NO
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**Goodyear**

**A00**

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